

Rocket BSW 11.6" Schematic Braswell

2015-11-09
REV : A00

DY : None Installed
OSP/1SP : different config for storage and DRAM
Drax : stuff on Drax

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Rocket BSW 11.6"

Rev
A00

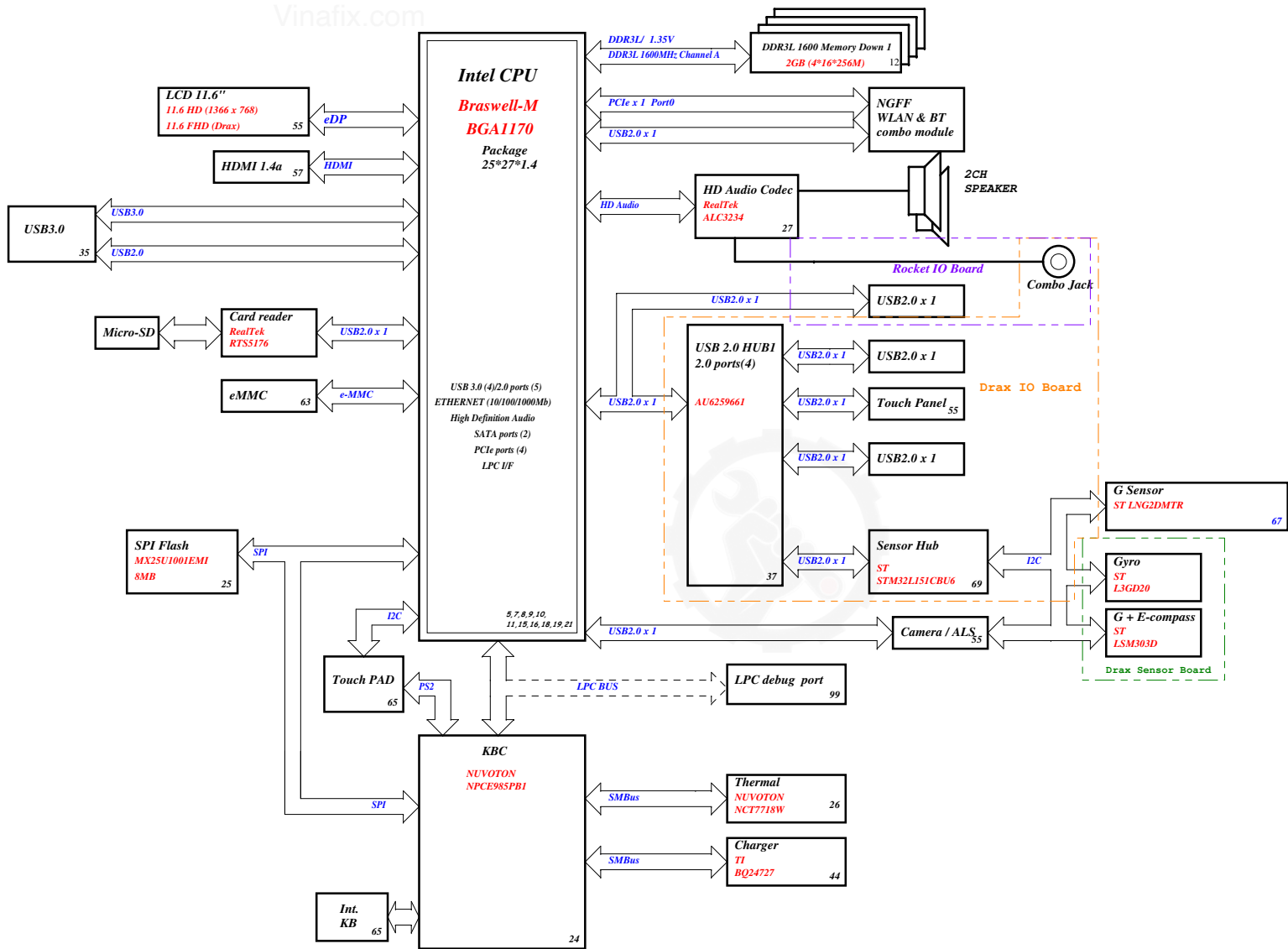
Date: Monday, November 09, 2015

Sheet 1 of 109

Project code : 4PD076010001
PCB P/N : 15235
Revision : -1

Rocket 11.6" Block Diagram - 0SP

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CHARGER	
BQ24727R6RR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+
SYSTEM DC/DC	
SY8288CRAC	45
SY8286BRAC	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5
	5V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	6FX_CORE
SYSTEM DC/DC	
SY8286RAC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5
Step Down Regulator	
SYW232DFC	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
SYSTEM DC/DC	
SY8286RAC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM DC/DC	
APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0
Step Down Regulator	
SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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SSID = CPU

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Date: Monday, November 09, 2015		Sheet 3 of	109


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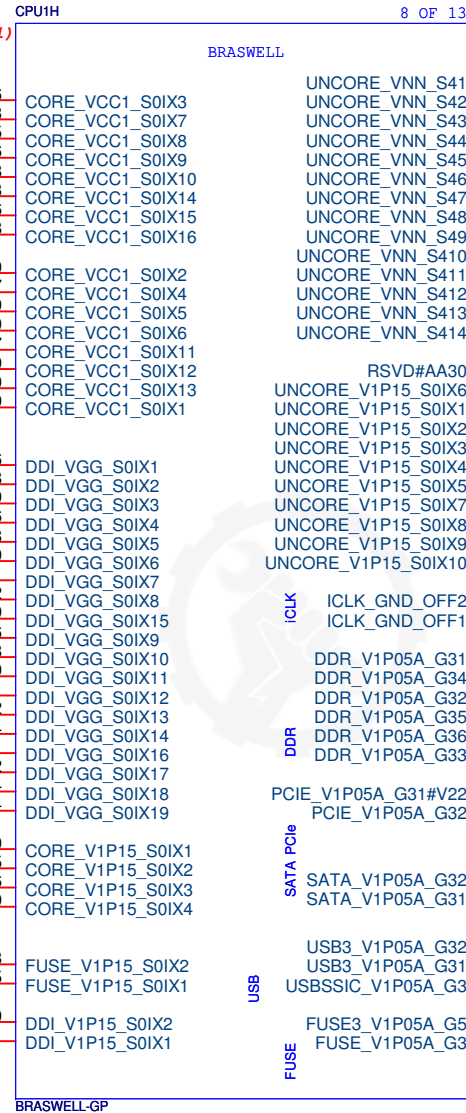


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A4	Rocket BSW 11.6"				A00
Date: Monday, November 09, 2015		Sheet 6		of 109	

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Imax=6.4A (merged VCC0+VCC1)

1V_CPU_CORE

1V_CPU_CORE

GFX_CORE

Imax=11A

1D15V_S5

Imax=0.7A (1D15V_S5)

1D15V_S5

1D15V_S5

1D05V_S5

Imax=1.9A (1D05V_S5)

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

1D05V_S5

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Title

CPU (VCC CORE)

Size

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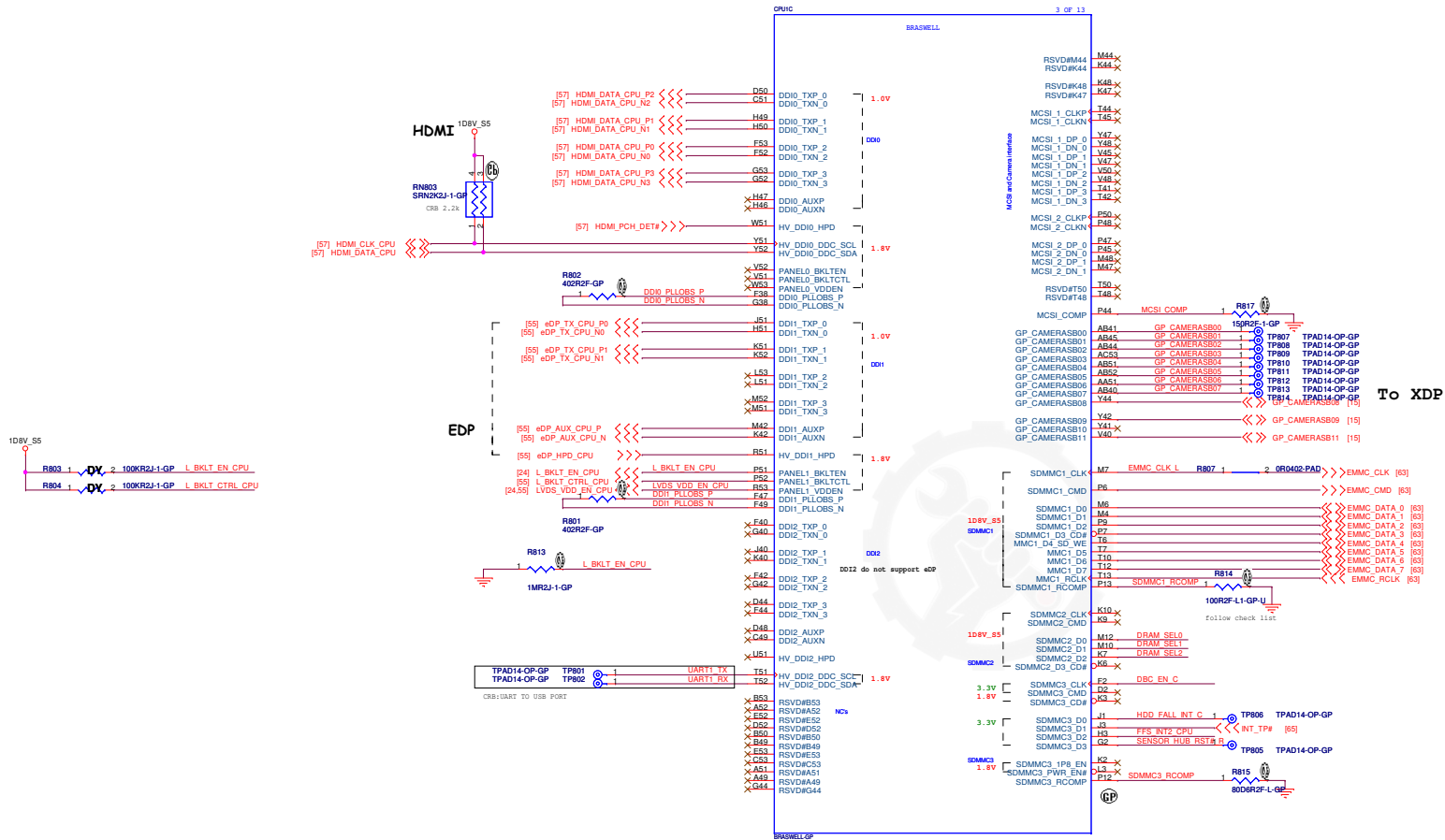
Rev

Rocket BSW 11.6"

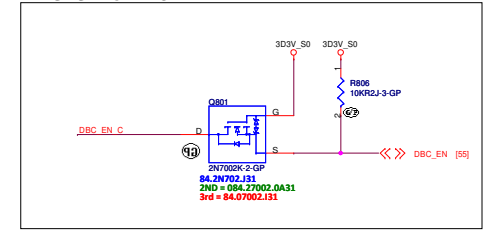
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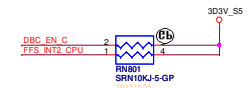
Sheet 7 of 109



Level Shift

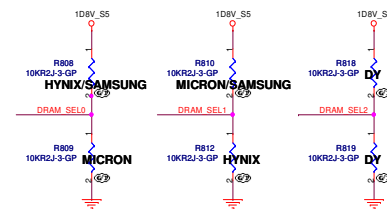


To XDP



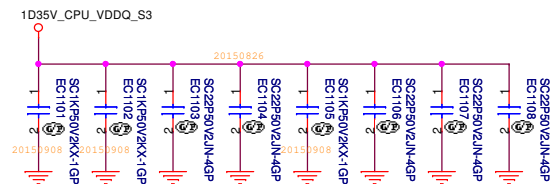
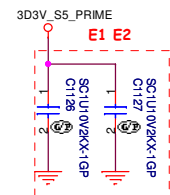
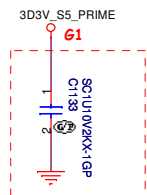
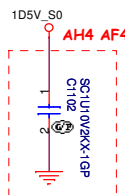
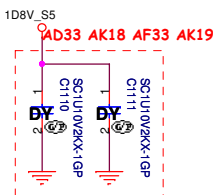
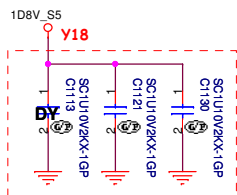
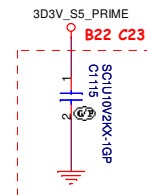
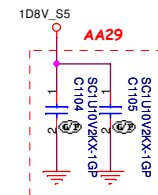
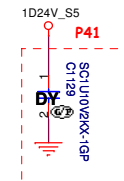
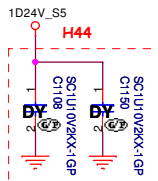
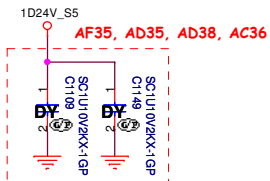
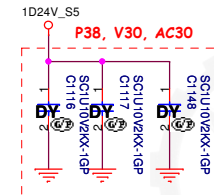
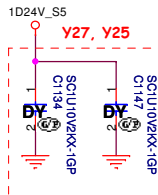
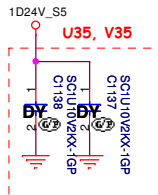
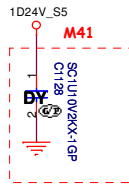
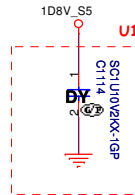
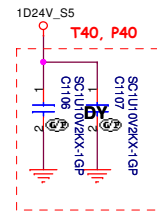
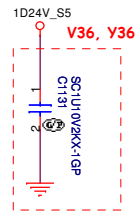
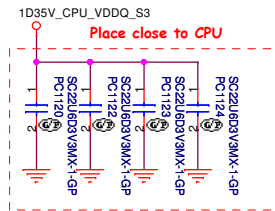
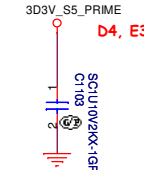
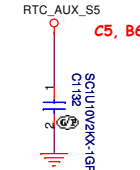
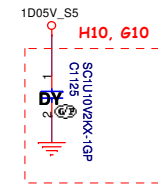
RAM ID bit order is DRAM_SEL2(Reserved), DRAM_SEL1,DRAM_SELO

Vender	RAM ID	Wistron PN	Mfr. PN	Capacity	Freq
So-DIMM	X00				
Hynix	X01	NX80R\$AB	H5TC4G63CFR-PBA	2G	1600MHZ
Micron	X10	NX80R\$CA	MT41K256M16HA-125:E	2G	1600MHZ
Samsung	X11	NX80R\$BC	K4B4G1646E-BYK0	2G	1600MHZ



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SSID = CPU

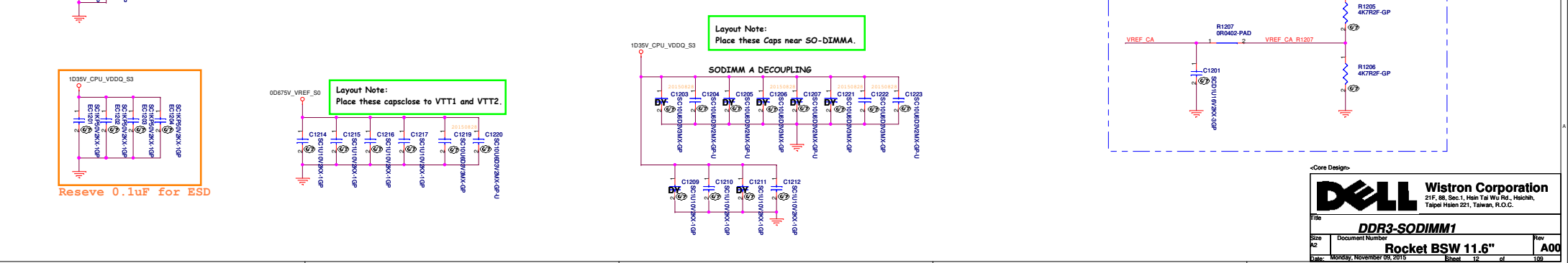
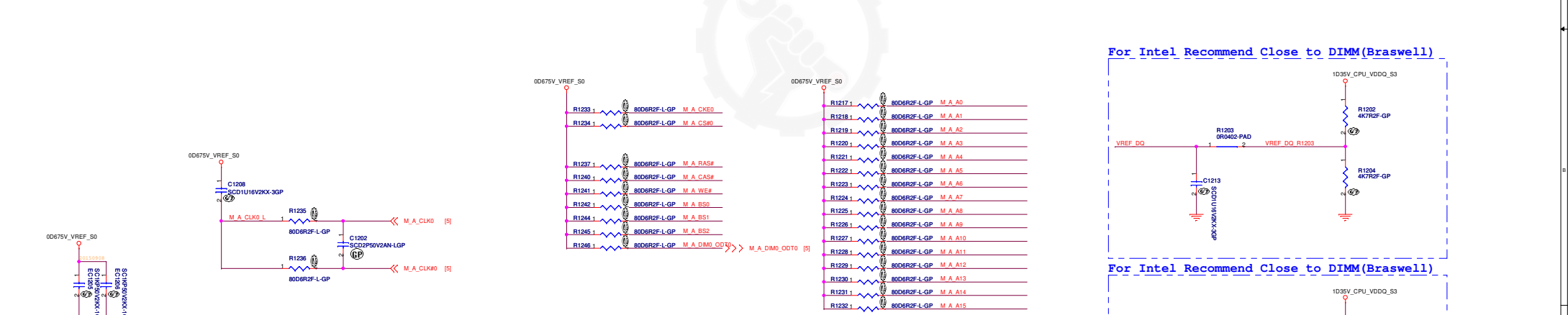
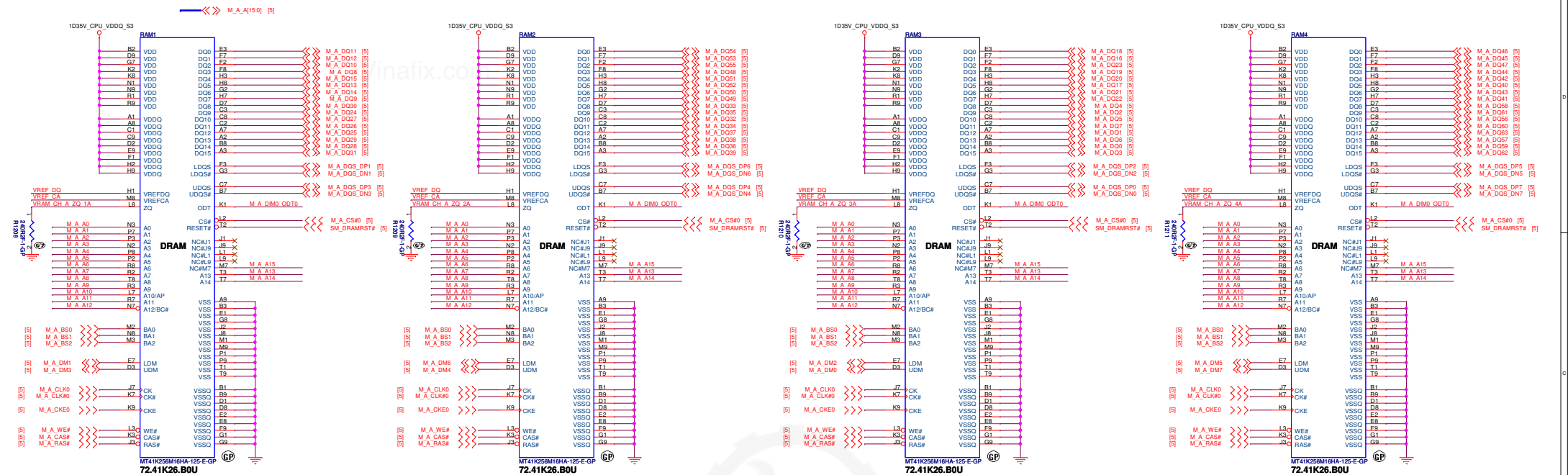


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Title			
CPU (Power CAP2)			
Size	Document Number	Rev	
A3	Rocket BSW 11.6"	A00	
Date:	Monday, November 09, 2015	Sheet	11 of 109

SSID = MEMORY



SSID = MEMORY

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Date: Monday, November 09, 2015			Sheet	14	of 109


SSID = CPU

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SSID = PCH


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Sheet 22 of 109

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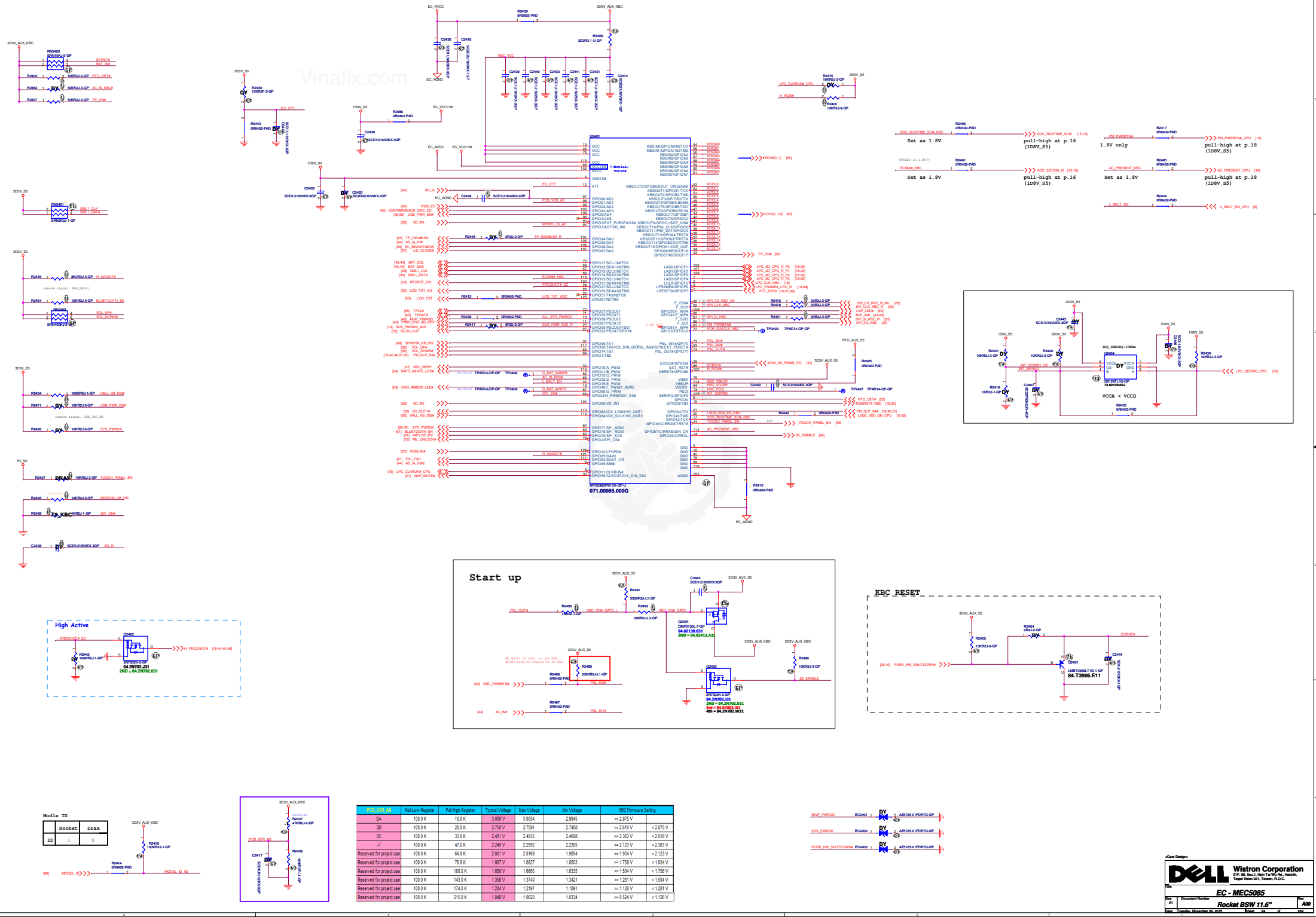
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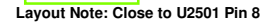
Sheet 23 of 109

SSID = KBC



Pin	With Alt	Pull/Up Register	Pull/Up Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.975 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7400	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4955	2.4680	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.894 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.887 V	1.8927	1.8503	>= 1.758 V	< 1.924 V
Reserved for project use	100.0 K	100.0 K	1.850 V	1.8595	1.8335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.350 V	1.3740	1.3421	>= 1.201 V	< 1.594 V
Reserved for project use	100.0 K	174.0 K	1.284 V	1.2987	1.2597	>= 1.126 V	< 1.594 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0254	>= 0.524 V	< 1.126 V

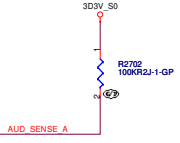
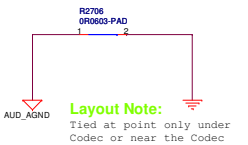
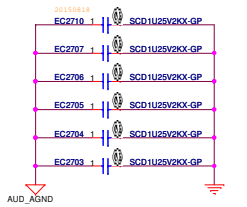
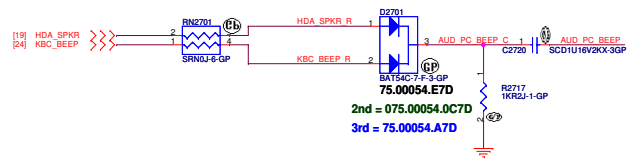
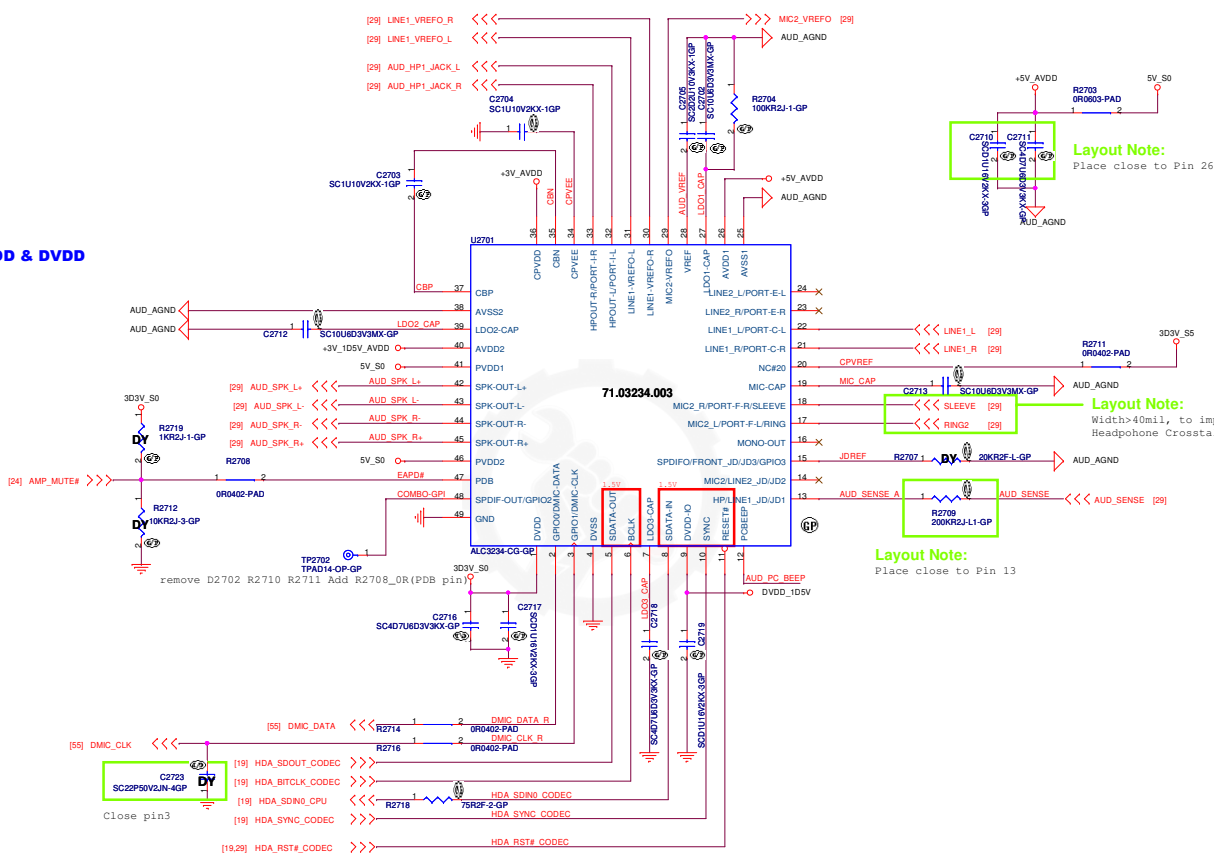
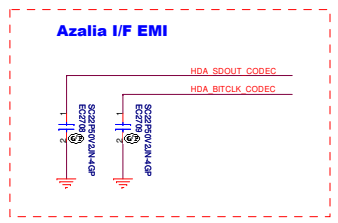
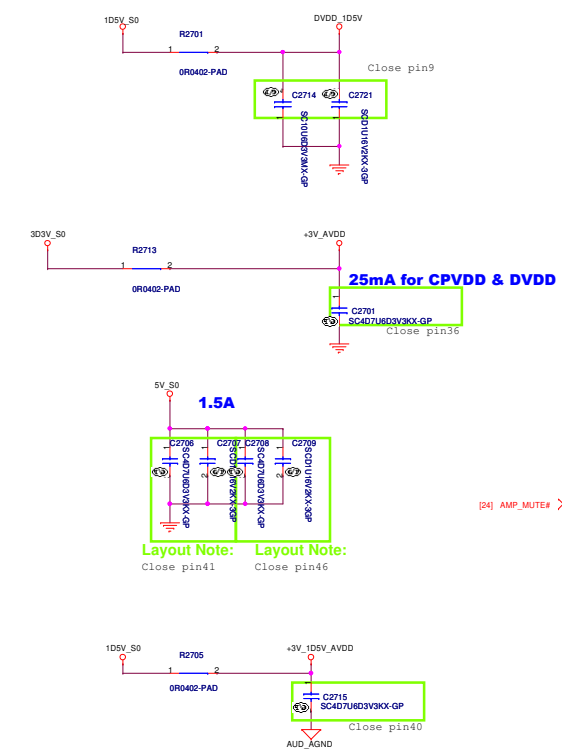
SPI FLASH ROM (8M byte) for CPU



Layout Note: Near Close

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

[illegible]



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Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 28 of 109

SSID = LOM

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Rev

A00

Date: Monday, November 09, 2015


Sheet 30 of 109

SSID = LAN

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Document Number

Rocket BSW 11.6"

Rev

A00

Date: Monday, November 09, 2015


Sheet 31 of 109

SSID = LAN CONN

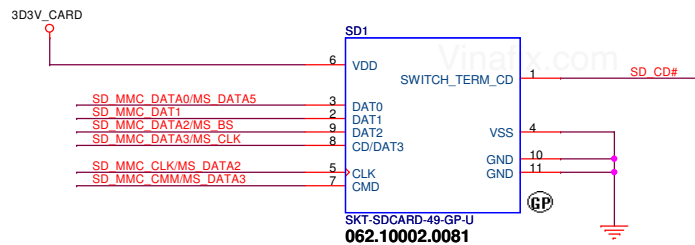
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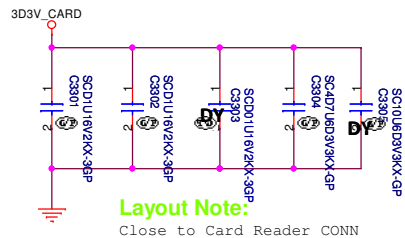
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Title (Reserved)RJ45+Transformer		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 32 of 109

SSID = Card Reader



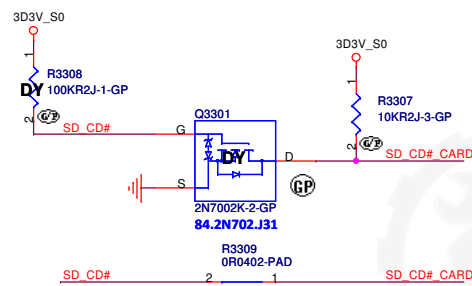
SD Card Connector

Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND

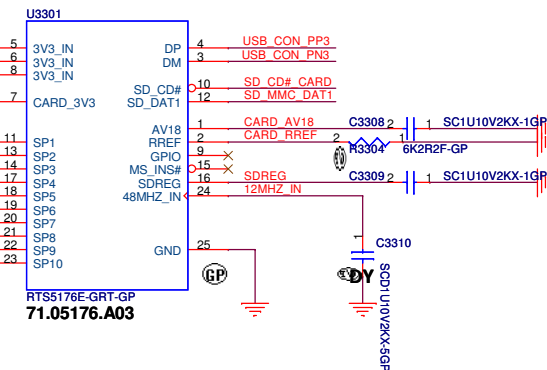
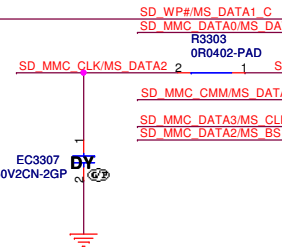


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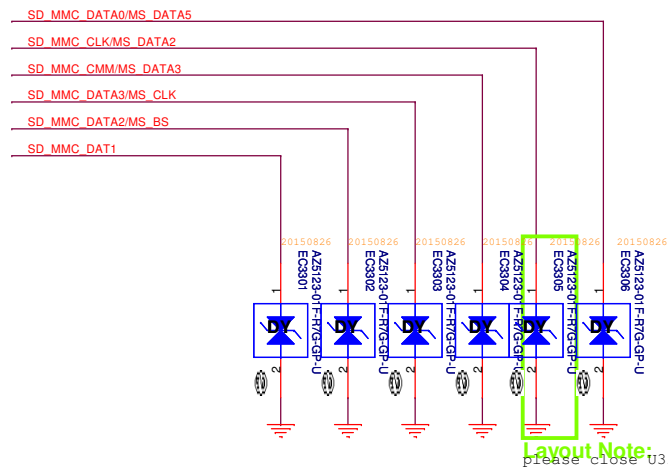
Close to Card Reader CONN



R3311
0R0402-PAD
20151015



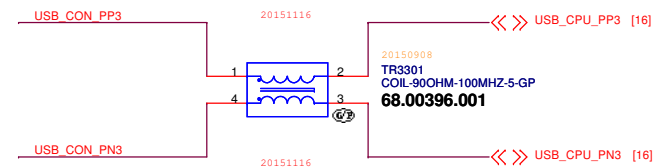
For EMI Reserved



Layout Note:

please close U3201

Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



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Card Reader + CONN

Title
 Size A3 Document Number **Rocket BSW 11.6"** Rev **A00**
 Date: Monday, November 16, 2015 Sheet 33 of 109

SSID = USB

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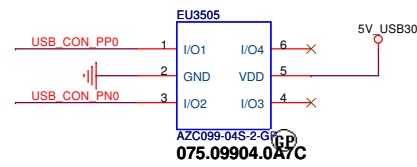
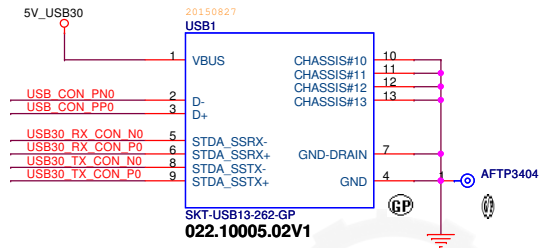
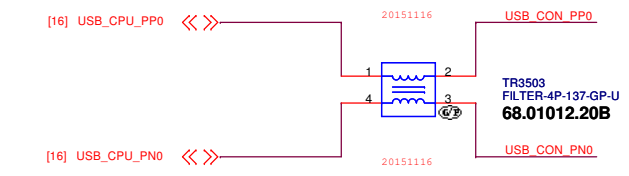
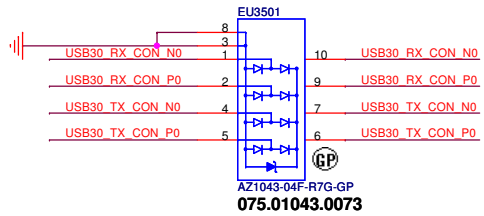
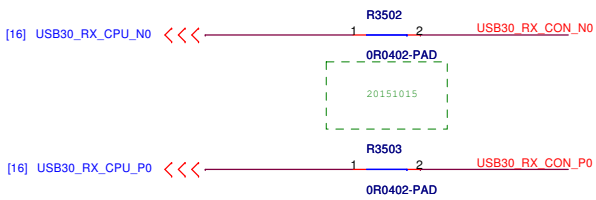
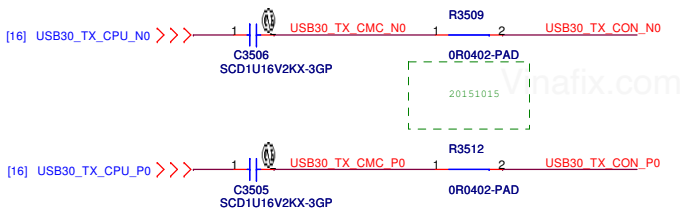
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Title
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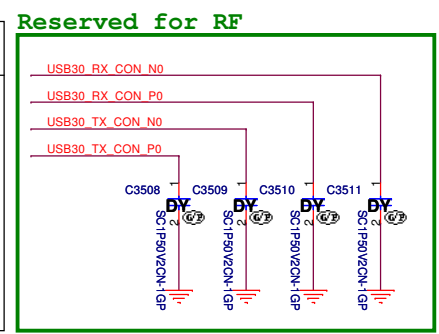
Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 34 of 109

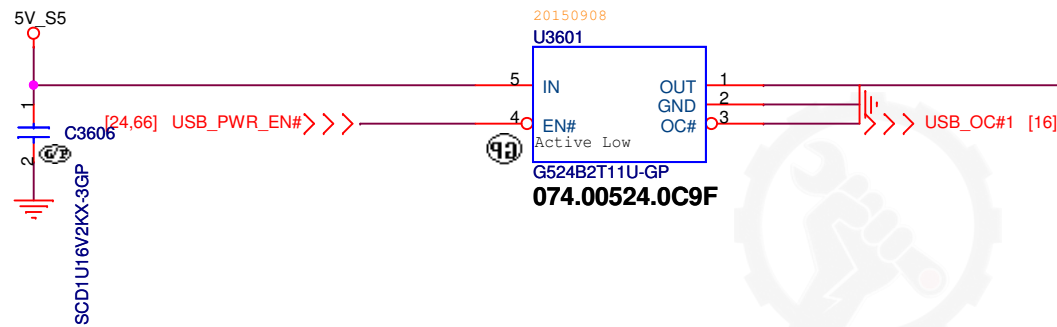
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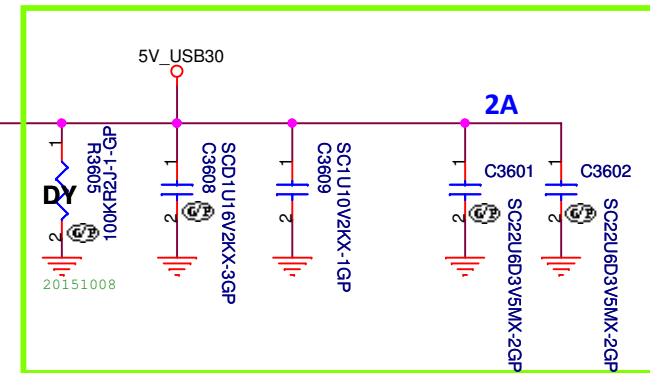
USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



USB3.0 Port1



Layout Note: Close CON1



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Title

USB Power SW

Size
A4

Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 36 of 109


SSID = USB

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Title			
USB2.0 HUB			
Size	Document Number		Rev
A4	Rocket BSW 11.6"		A00
Date: Monday, November 09, 2015		Sheet 37 of	109

Blanking



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Size
A4

Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 38 of 109

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Size
A4

Document Number

Rocket BSW 11.6"

Rev

A00

Date: Monday, November 09, 2015

Sheet 39 of 109

Blanking

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Document Number

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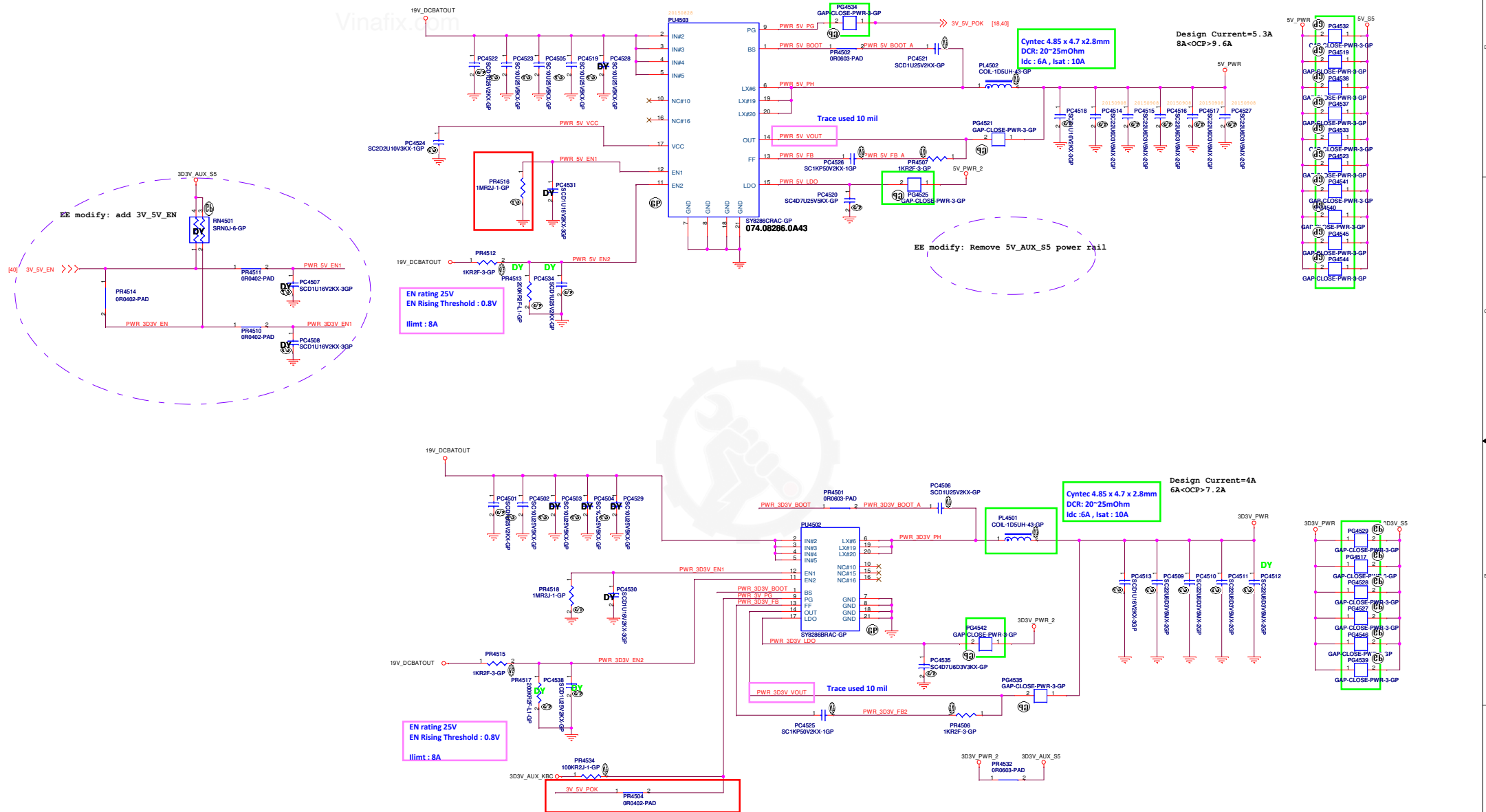
Date: Monday, November 09, 2015

Sheet 41 of 109

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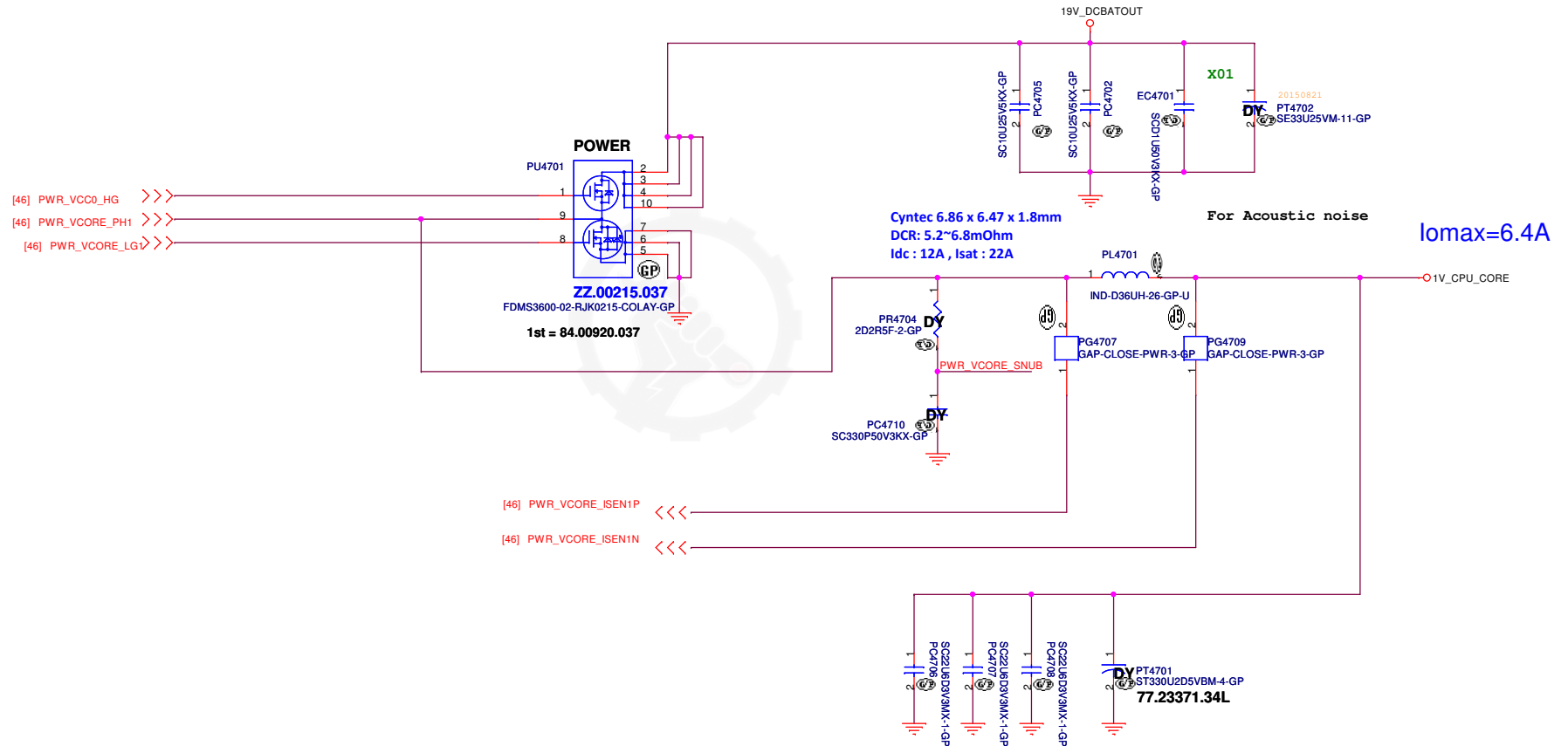
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Title (Reserved)			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 42 of	109



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SSID = CPU Regulator

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Title		NCP81201MNTXG CPUCORE(2/3)	
Size	Document Number	Date	Rev
A3		Monday, November 09, 2015	A00
Rocket BSW 11.6"		Sheet	47 of 109

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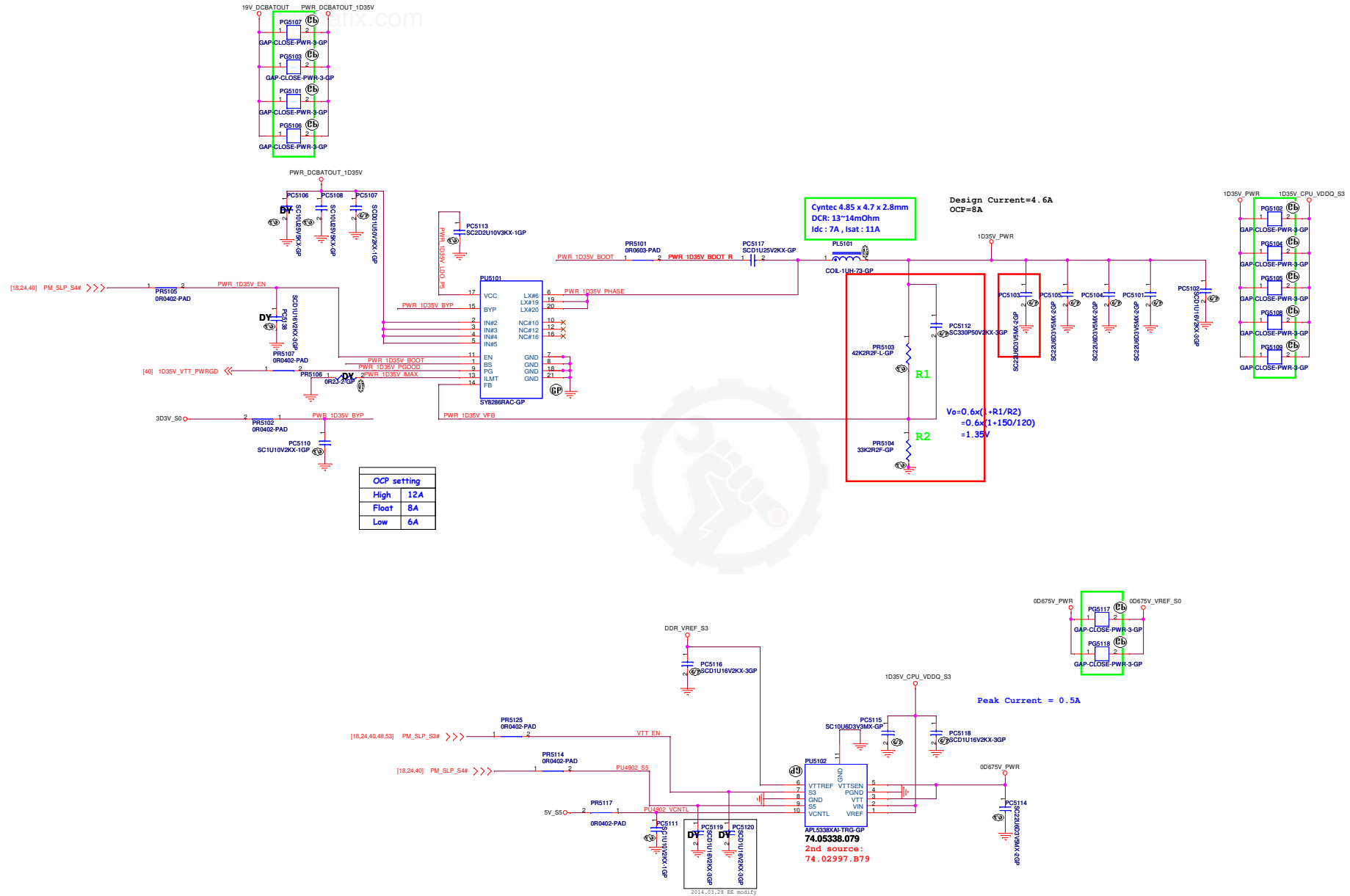
Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 49 of 109

SY8206D for 1D35V

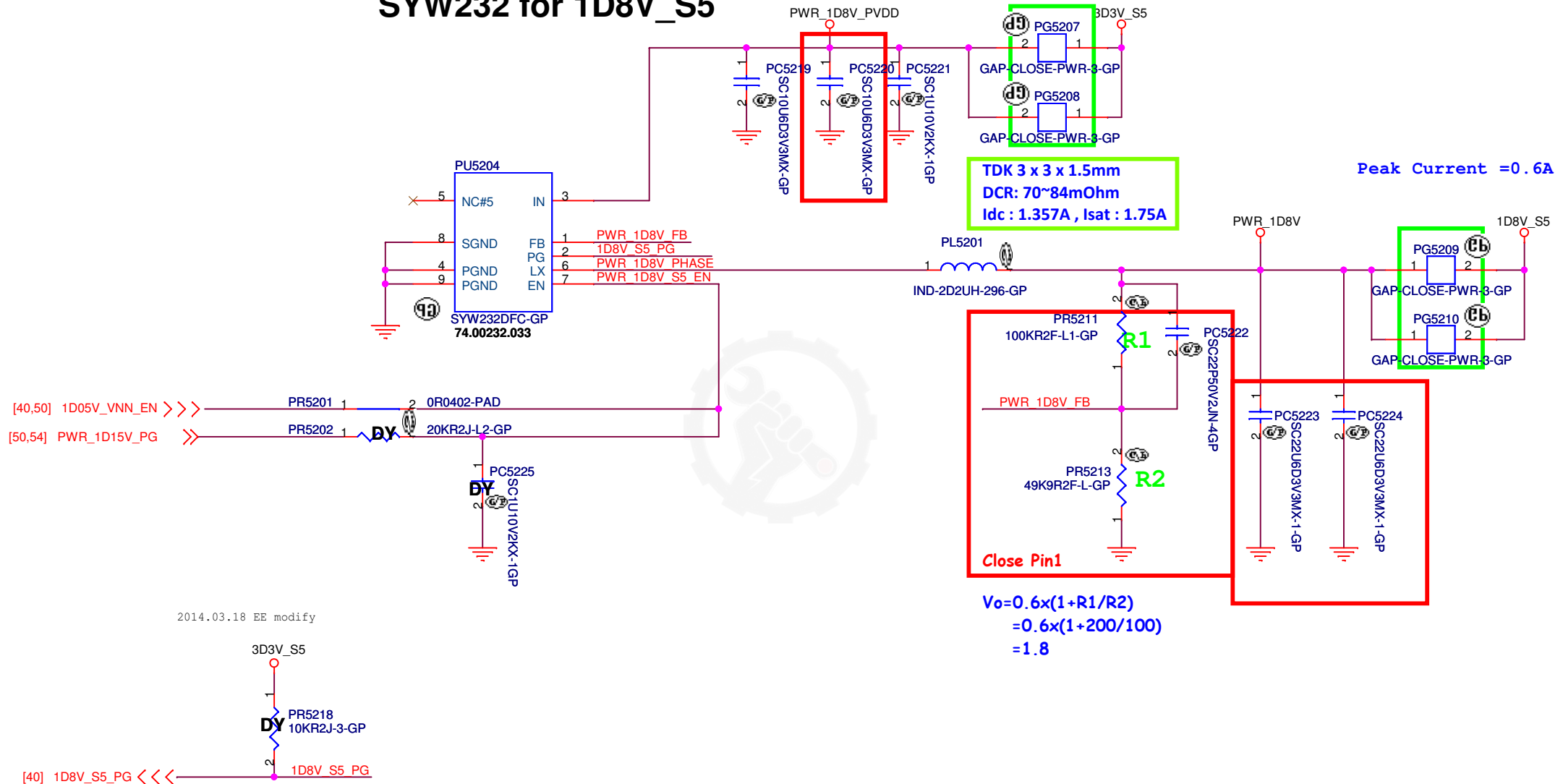


<Core Design>

SSID = PWR.Plane.Regulator_1p8v

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SYW232 for 1D8V_S5



<Core Design>

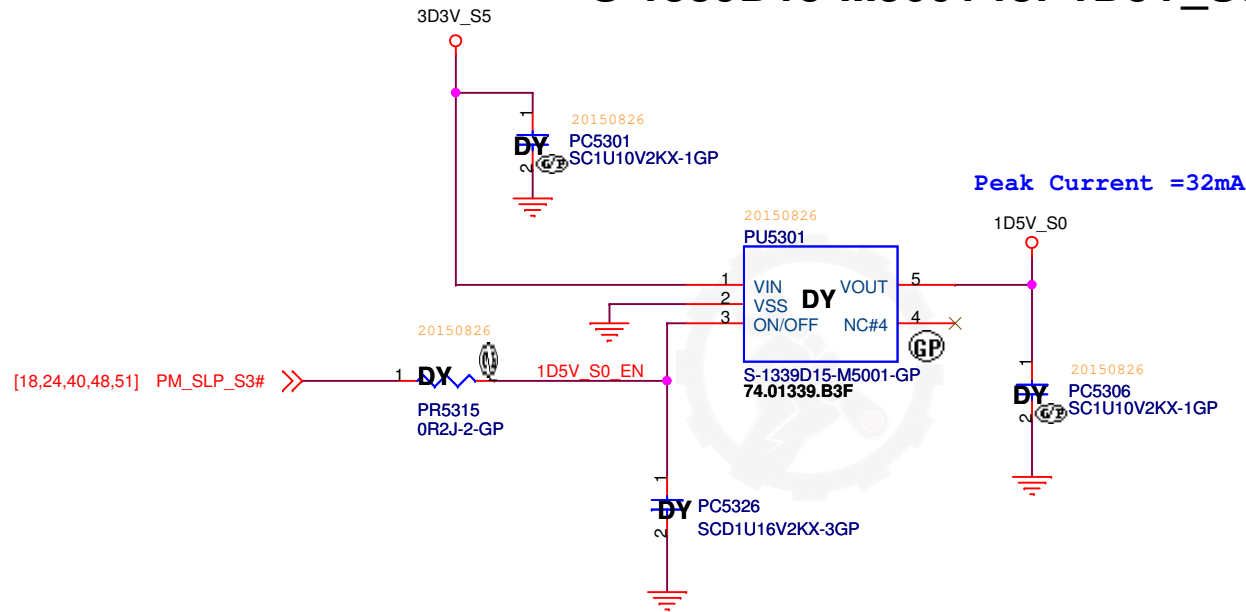


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Title			SYW232DFC_1D8V	
Size	Document Number	Rocket BSW 11.6"		Rev
A4				A00
Date: Monday, November 09, 2015		Sheet	52	of 109

S-1339D15-M5001 for 1D5V_S0



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Title

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Size
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Document Number

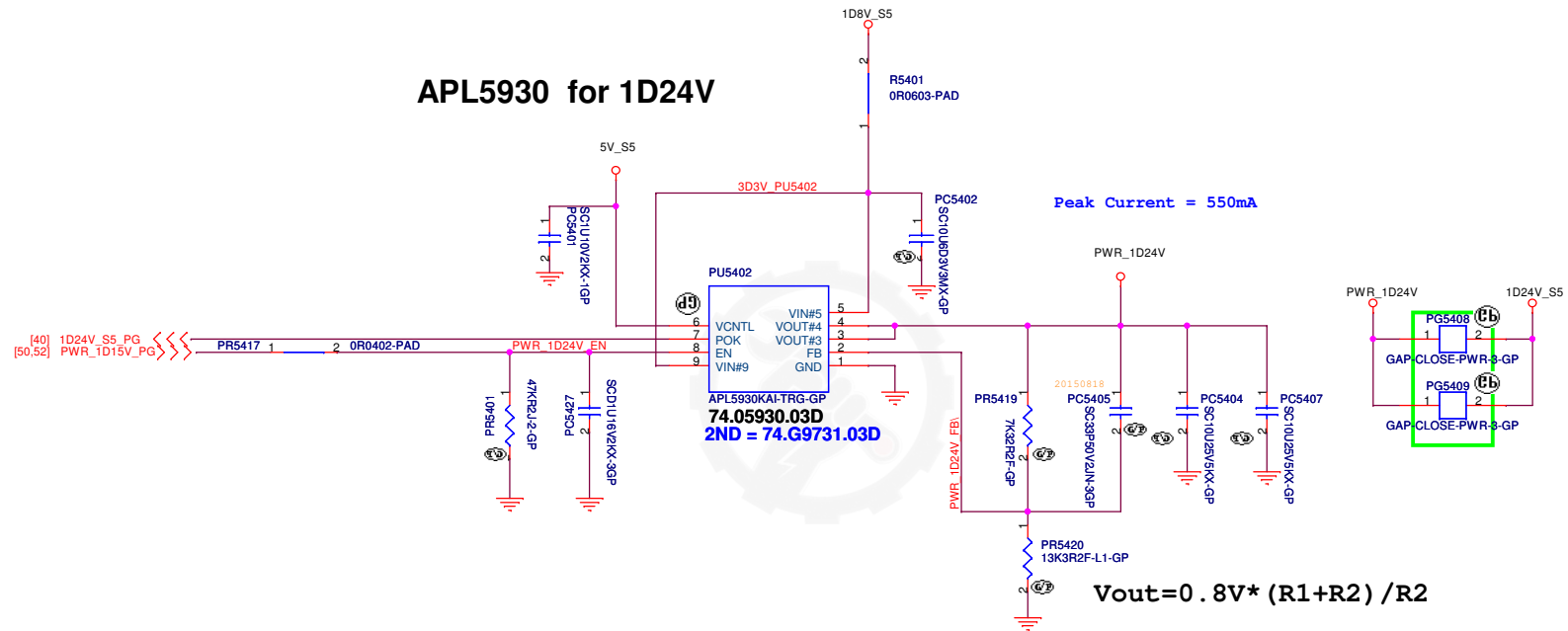
Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 53 of 109

APL5930 for 1D24V



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Title

APL5930_1D24V

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Document Number

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Rev

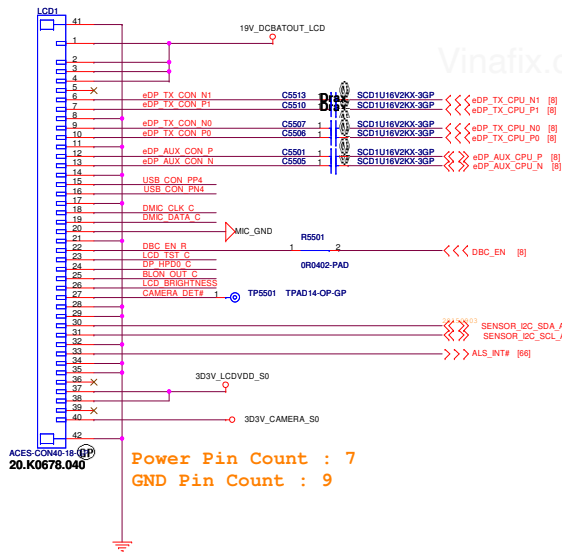
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Date: Monday, November 09, 2015

Sheet 54 of 109

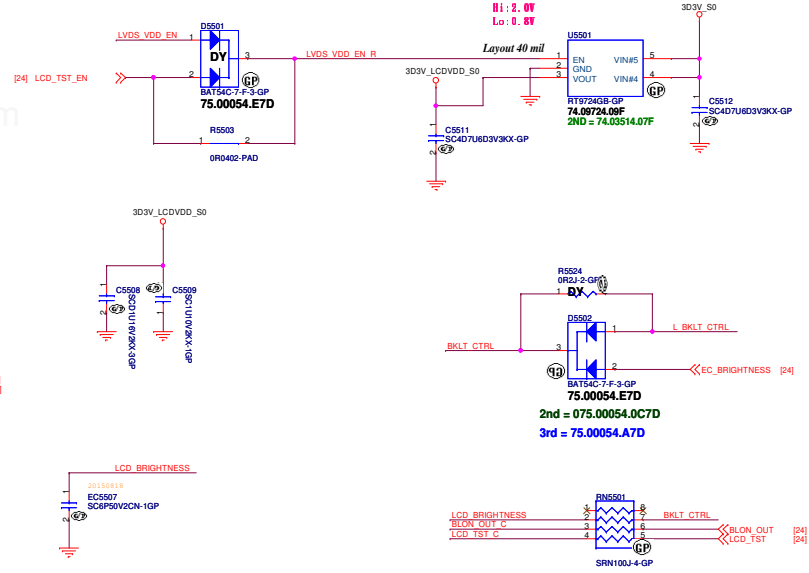
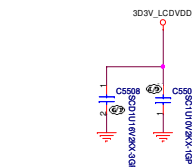
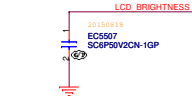
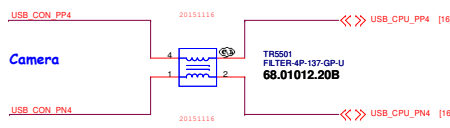
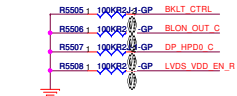
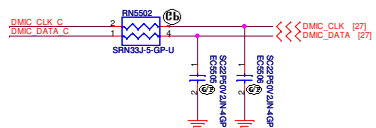
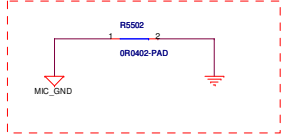
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Panel Conn.

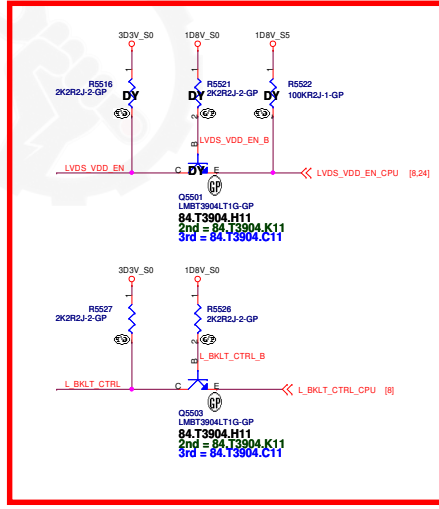


Power Pin Count : 7
GND Pin Count : 9

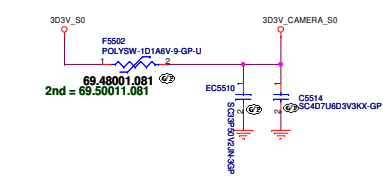
Layout: Close CONN LCD1



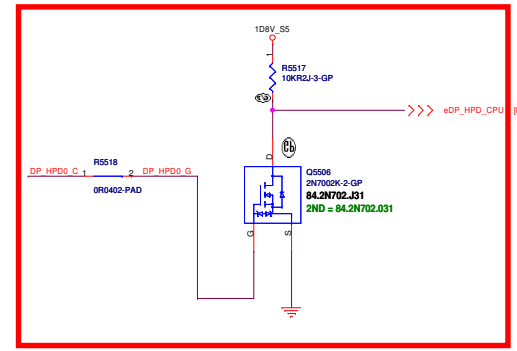
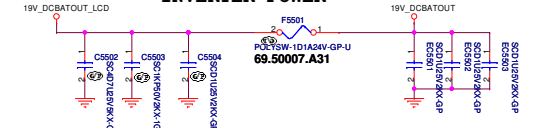
Level shift



CAMERA POWER



INVERTER POWER



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Title

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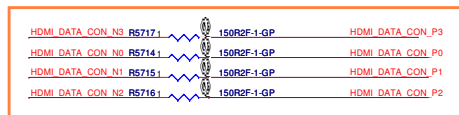
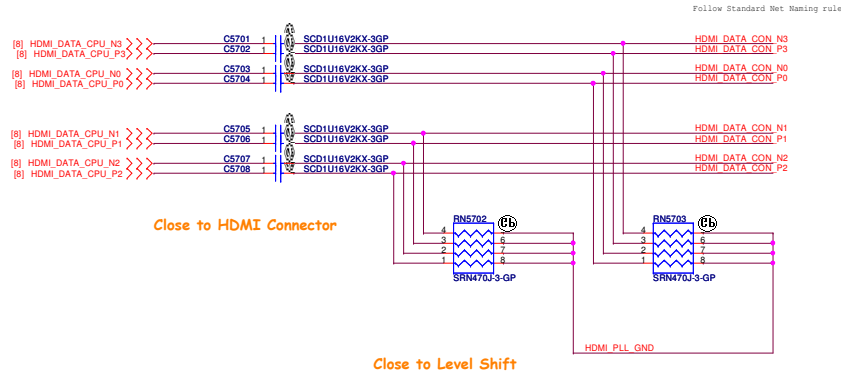
Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 56 of 109

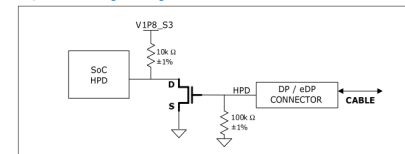
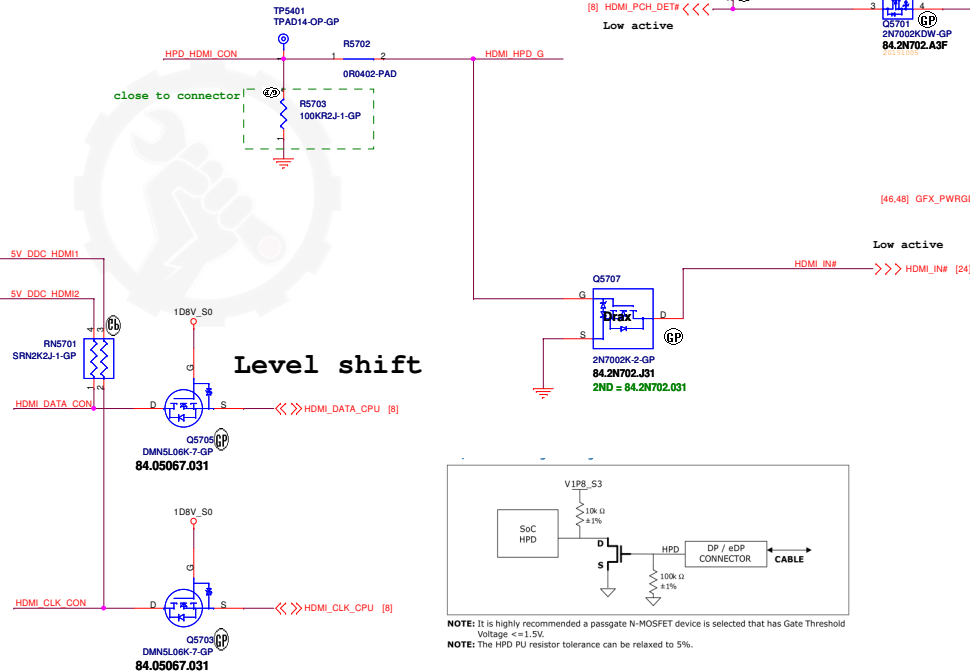
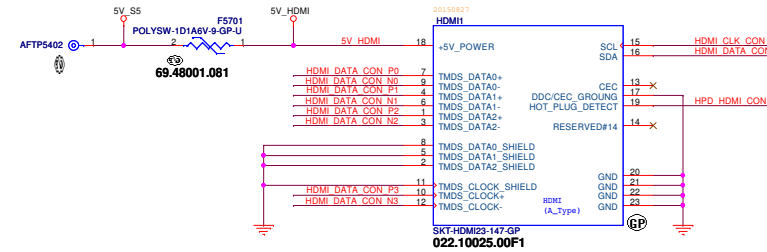
HDMI Level Shifter & CONNECTOR



Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI



Reserve 0.1uF for ESD



NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <= 1.5V.
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms ±20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts


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SSID = Display Port

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Title (Reserved) Display Port		
Size	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 58 of 109


SSID = DVI

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Title (Reserved) DVI			
Size	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 59 of	109

SSID = SATA

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Title HDD			
Size	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 60 of	109

SSID = WWAN

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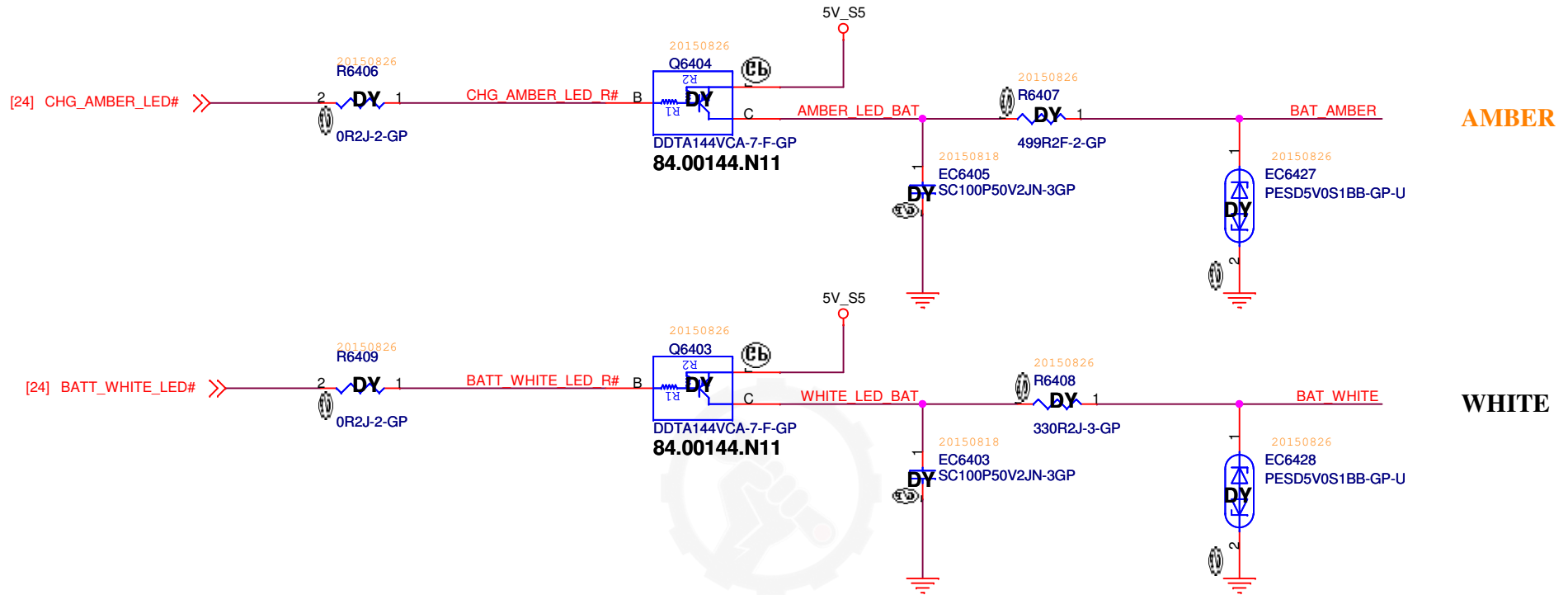
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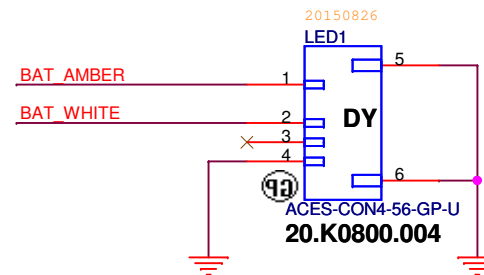
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Title (Reserved) WWAN			
Size	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 62 of	109

SSID = LED / PWRBTN

Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO



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Title

LED / PWRBTN

Size
A4

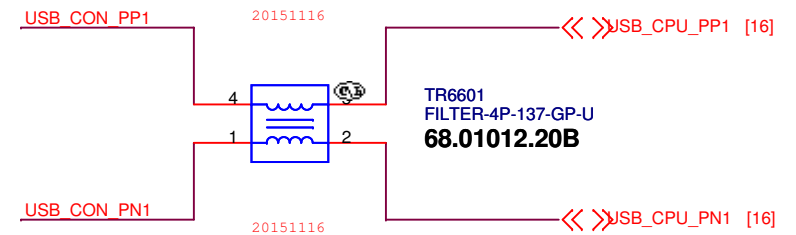
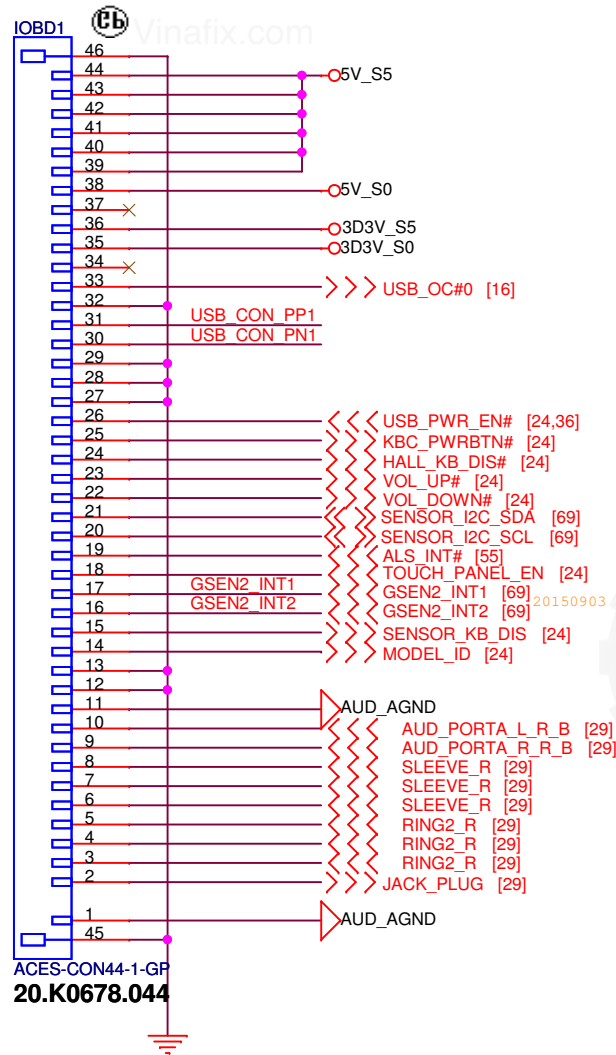
Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 64 of 109



Power Pin Count : 10
GND Pin Count : 5

USB3.0 Port2

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Title

IO Board CONN

Size
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Document Number

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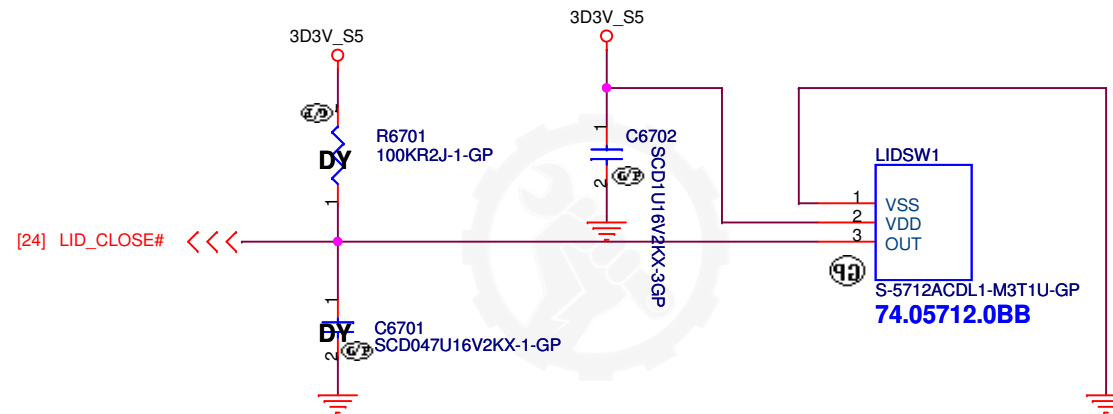
Rev

A00

Date: Monday, November 16, 2015

Sheet 66 of 109

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Title

Hall Sensor

Size
A4

Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 67 of 109

SSID = Debug CONN

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Title

(Reserved) Debug CONN

Size
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Document Number

Rocket BSW 11.6"

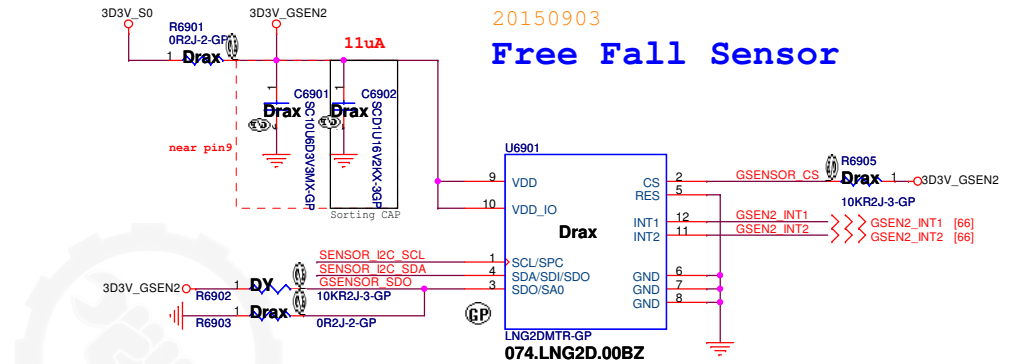
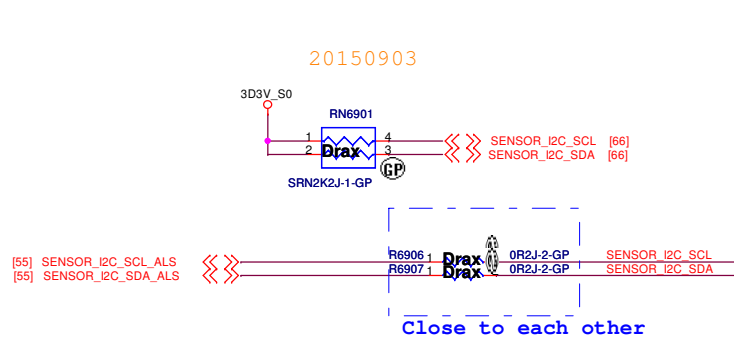
Rev
A00

Date: Monday, November 09, 2015

Sheet 68 of 109

SSID = Sensor

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Title			
Sensor			
Size	Document Number	Rev	
A3	Rocket BSW 11.6"	A00	
Date: Monday, November 09, 2015		Sheet	69 of 109

SSID = Free Fall Sensor

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Title Free Fall Sensor		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 70 of 109

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Title (Reserved)Thunderbolt (1/5)		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 71 of 109

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Title (Reserved)Thunderbolt (2/5)			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date:	Monday, November 09, 2015	Sheet 72 of	109

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Title (Reserved)Thunderbolt (3/5)		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 73 of 109

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Title (Reserved)Thunderbolt (4/5)			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015	Sheet	74 of	109

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Title (Reserved)Thunderbolt (5/5)		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 75 of 109

Blanking

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Title **(Reserved)GPU (1/5) PEG**

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Title **(Reserved)GPU (2/5) DIGITAL**


Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 77 of 109

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Title (Reserved)GPU (3/5) VRAM			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date:	Monday, November 09, 2015	Sheet 78 of	109

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Title **(Reserved)GPU (4/5) GPIO**

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Title (Reserved)GPU (5/5) PWR/GND		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015		Sheet 80 of 109

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Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 81	of 109

Blanking

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Title **(Reserved)VRAM3,4 (2/4)**

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Title **(Reserved)VRAM5,6 (3/4)**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Title **(Reserved)VRAM7,8 (4/4)**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Title **(Reserved)VGA_CORE**

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Title **(Reserved)DISCRETE VGAPOWER**

Size	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 86 of 109

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Title

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Size
A4

Document Number

Rocket BSW 11.6"

Rev
A00


Date: Monday, November 09, 2015

Sheet 87 of 109

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Title (Reserved)			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 88 of	109

20150828

34.4YW18.001

SPRING-171-GP
SPR1



20150827

34.4YW18.001

SPRING-171-GP
SPR2



20150827

34.4YW18.001

SPRING-171-GP
SPR3



20151008

34.34S02.002

SPRING-98-GP
SPR4



20151008

34.34S02.002

SPRING-98-GP
SPR5



20151008

34.34S02.002

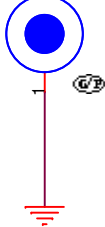
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20150901

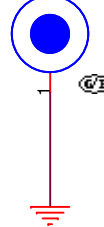
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H1
HOLE354R237-GP



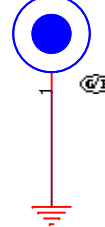
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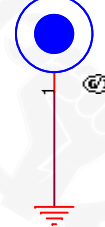
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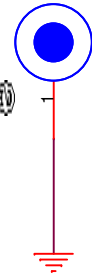
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20151012 Remove H12 H14

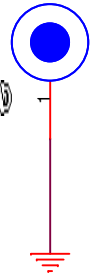
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HS1
STF237R117H67-3-GP



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HS2
STF237R117H67-3-GP



34.4OX45.101

HS3
STF237R117H67-3-GP



34.4OX45.101

HS4
STF237R117H67-3-GP



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Title UNUSED PARTS/EMI Capacitors		
Size A4	Document Number Rocket BSW 11.6"	Rev A00
Date: Monday, November 09, 2015 Sheet 89 of 109		

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Title **(Reserved)NFC Connector**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 90 of 109

Blanking



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Title

(Reserved) TPM

Size

A4

Document Number

Rocket BSW 11.6"

Rev

A00

Date: Monday, November 09, 2015

Sheet 91 of 109

Blanking



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Title **(Reserved)Finger Print**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Title			
(Reserved)Express Card			
Size A3	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015	Sheet	93	of 109

Blanking



<Core Design>

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Title <i>(Reserved)Smart Card Socket</i>			
Size A4	Document Number <i>Rocket BSW 11.6"</i>		Rev <i>A00</i>
Date: Monday, November 09, 2015		Sheet 94 of	109

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Title **(Reserved)SW GFX eDP**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 95 of 109

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Title

(Reserved)Bottom Docking

Size
A4

Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 96 of 109

Blanking



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Title **(Reserved)LAN**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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Date: Monday, November 09, 2015 Sheet 97 of 109

Blanking



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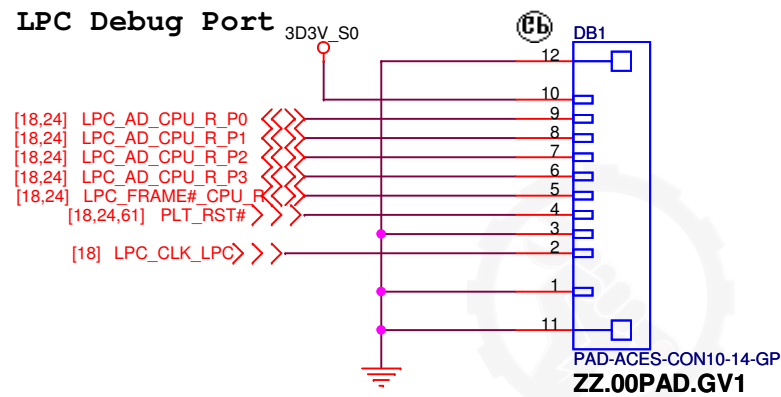
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **(Reserved)LAN SWITCH**

Size	Document Number	Rev
	Rocket BSW 11.6"	A00


SSID = DEBUG PORT

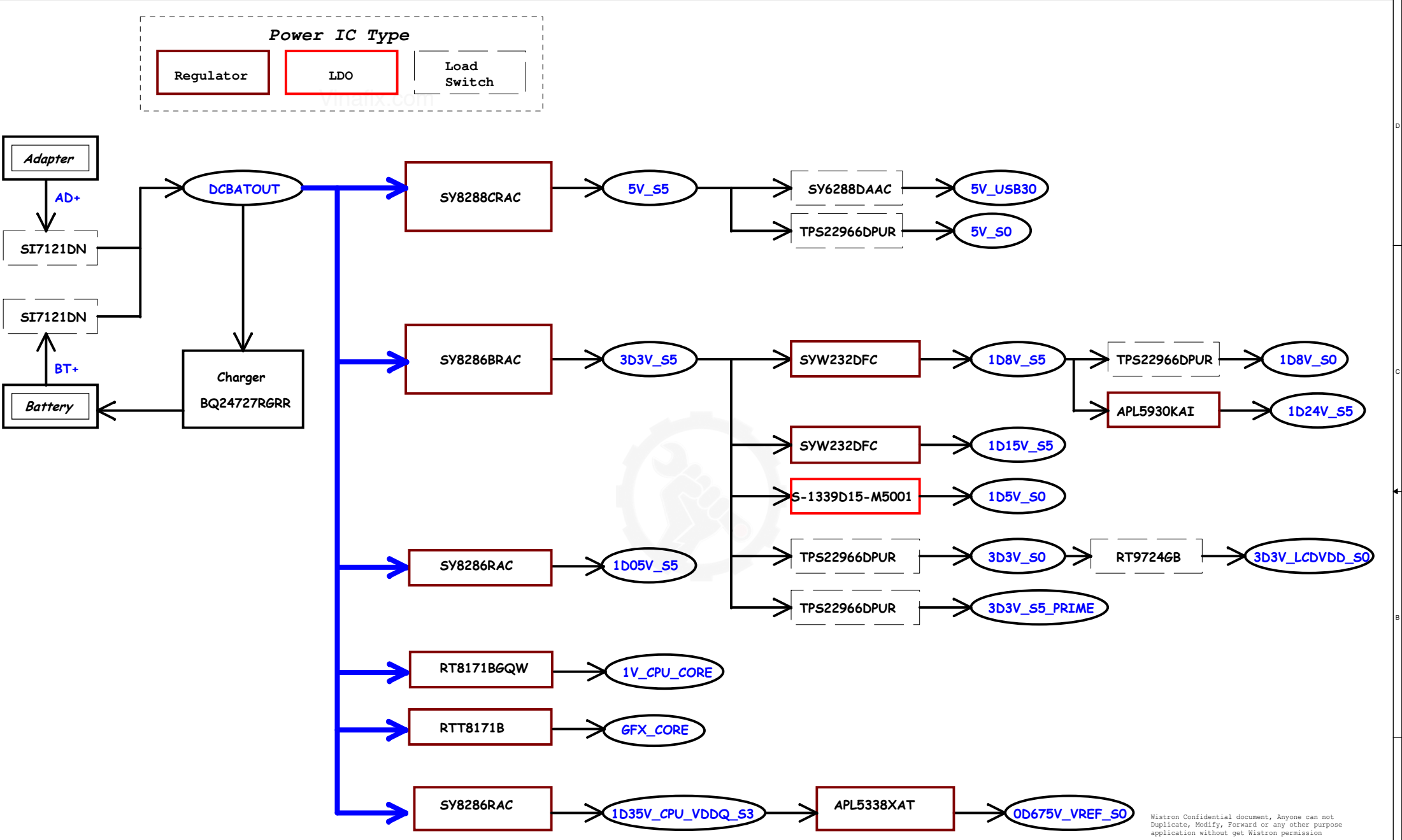
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20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

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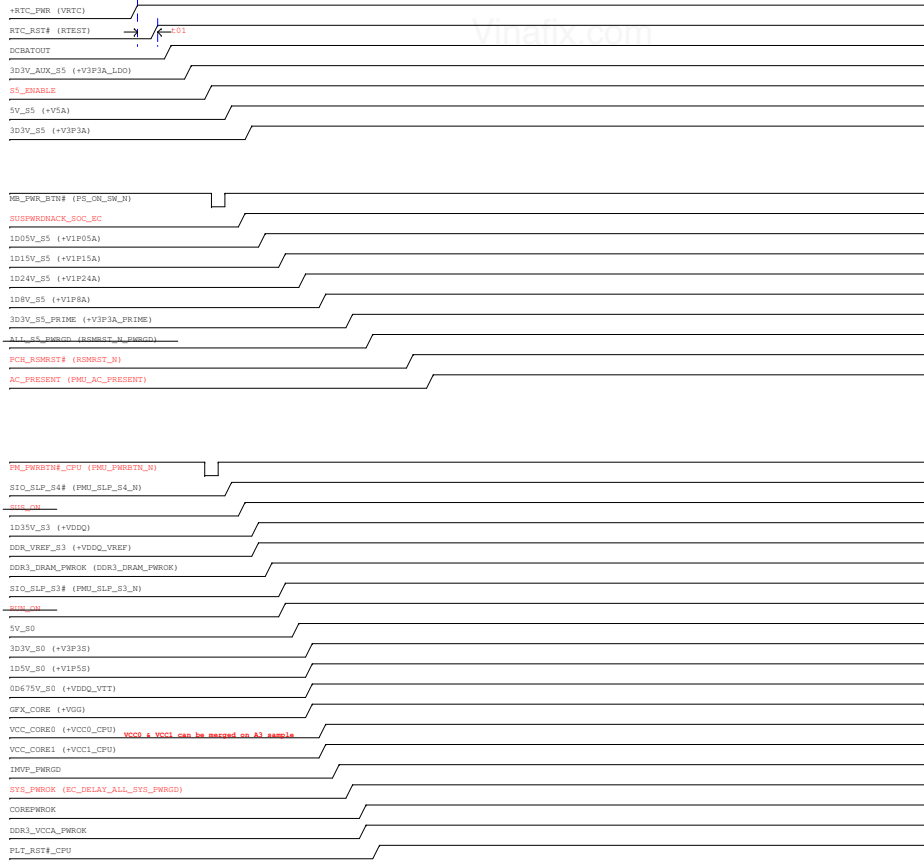
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Title CPU_XDP			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 16, 2015		Sheet 99 of 109	



Intel-Power Up Sequence

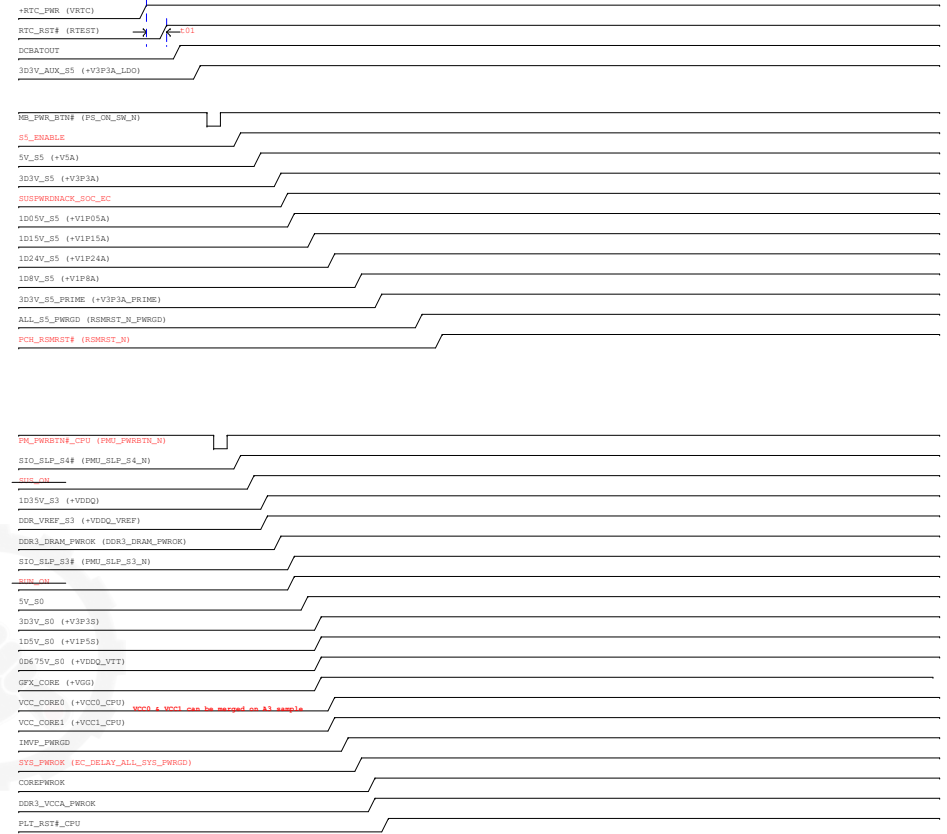
(AC mode) Red word : RBC QP10

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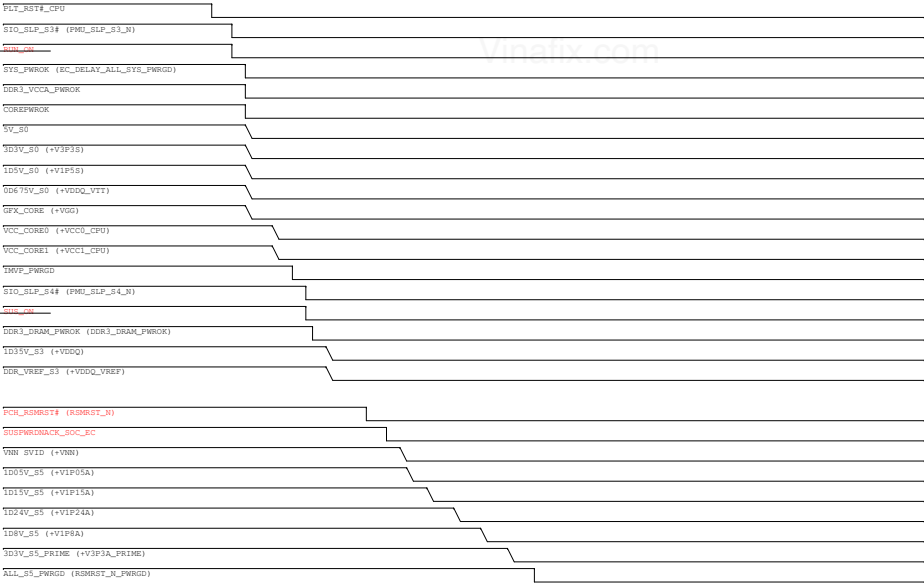
Intel-Power Up Sequence

(DC mode) Red word : RBC QP10



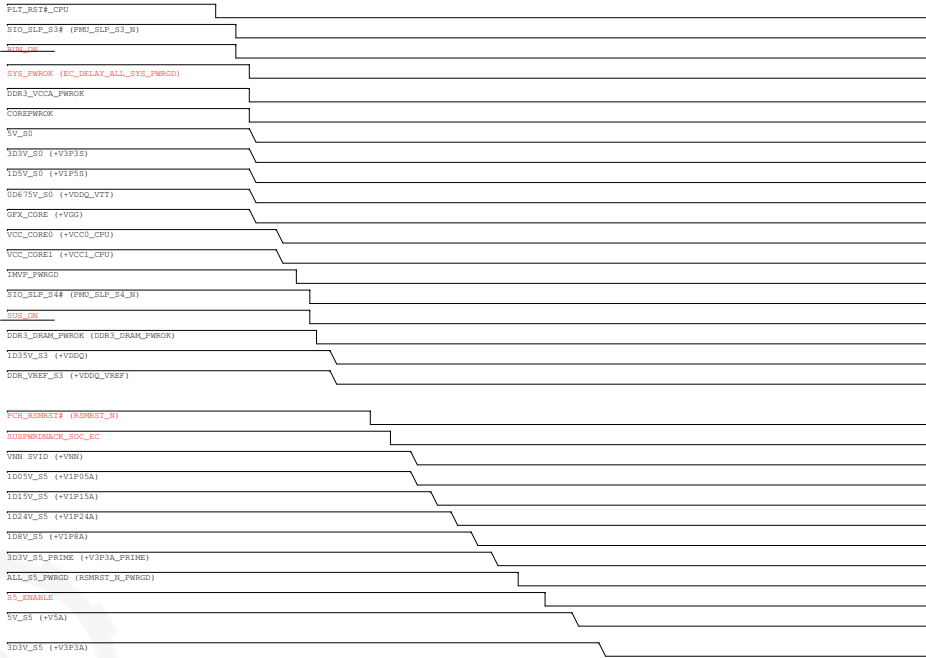
Intel-Power Down Sequence

(AC mode) Red word : X8C QP10



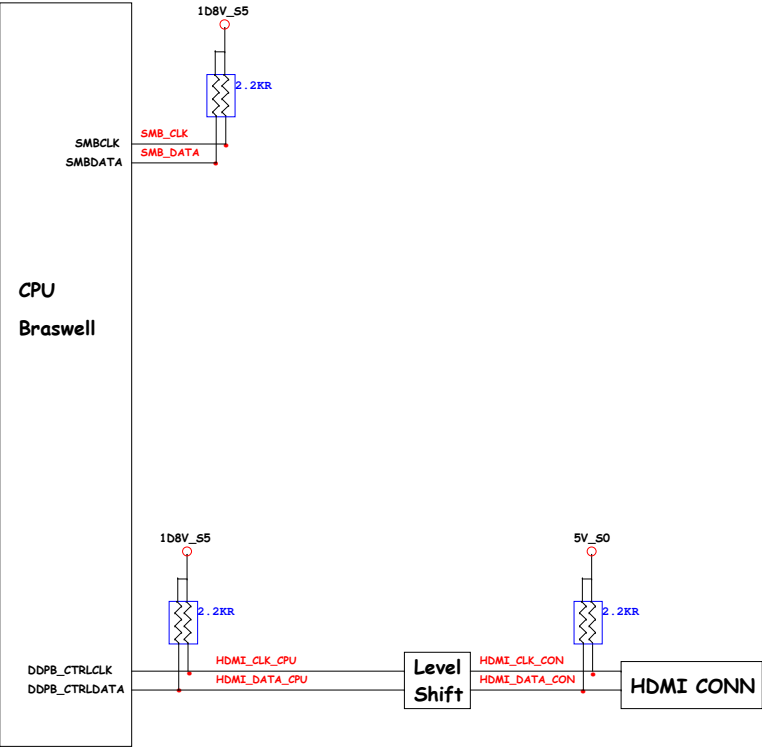
Intel-Power Down Sequence

(DC mode) Red word : X8C QP10

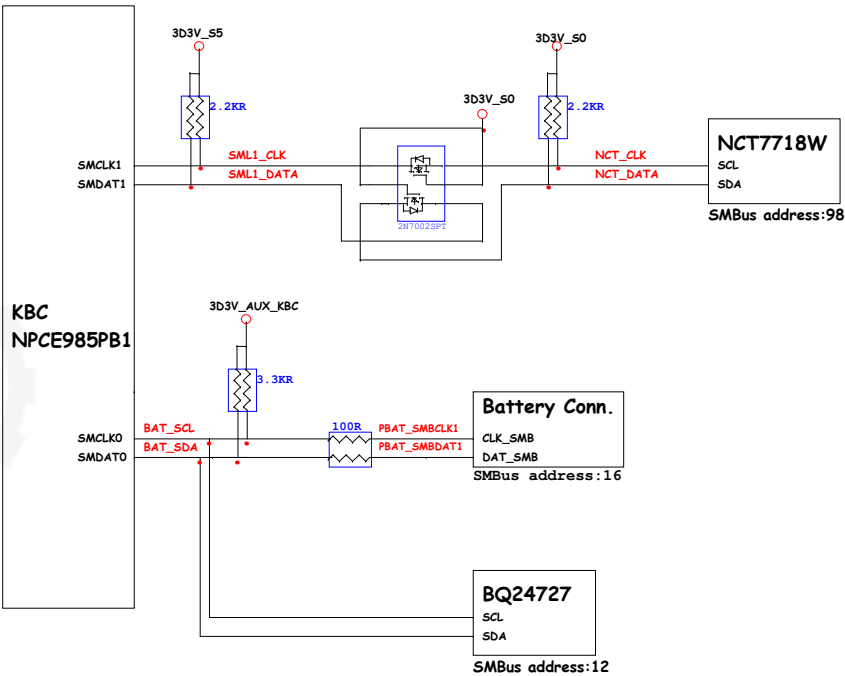


PCH SMBus Block Diagram

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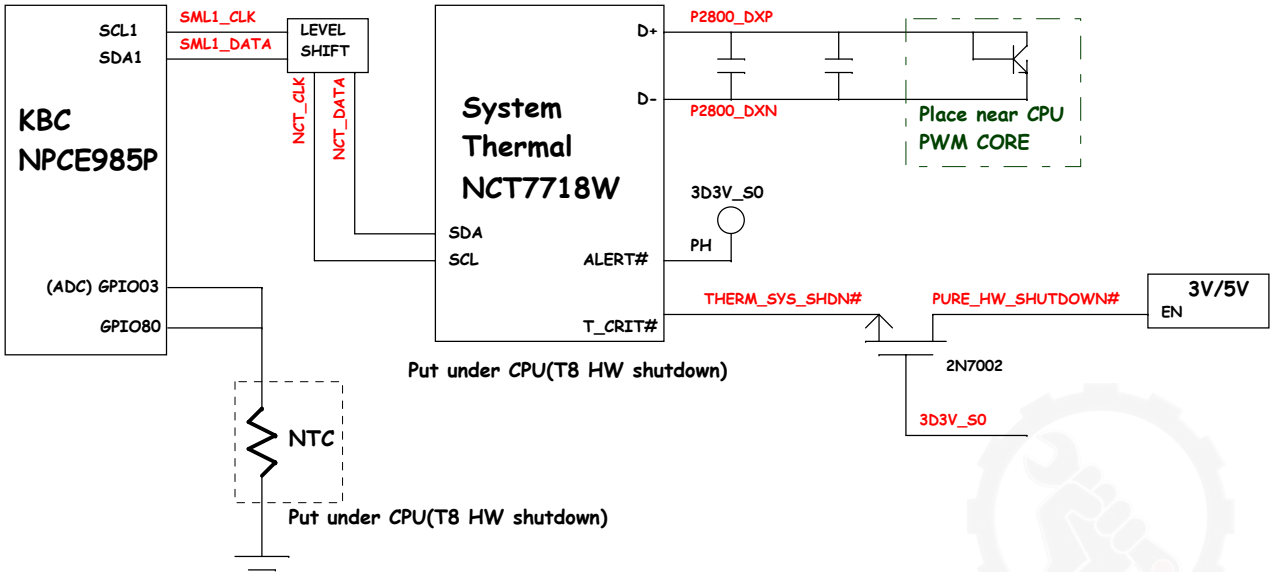


KBC SMBus Block Diagram

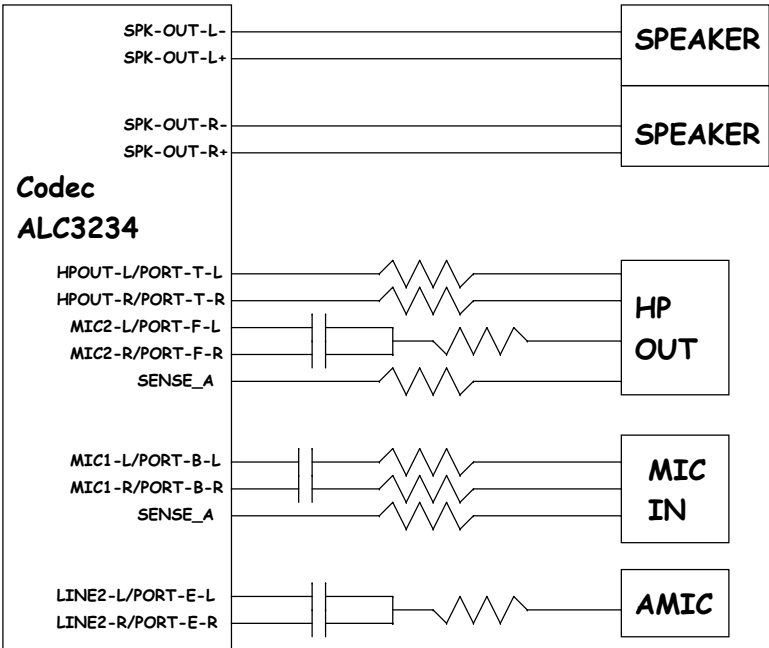


Thermal Block Diagram

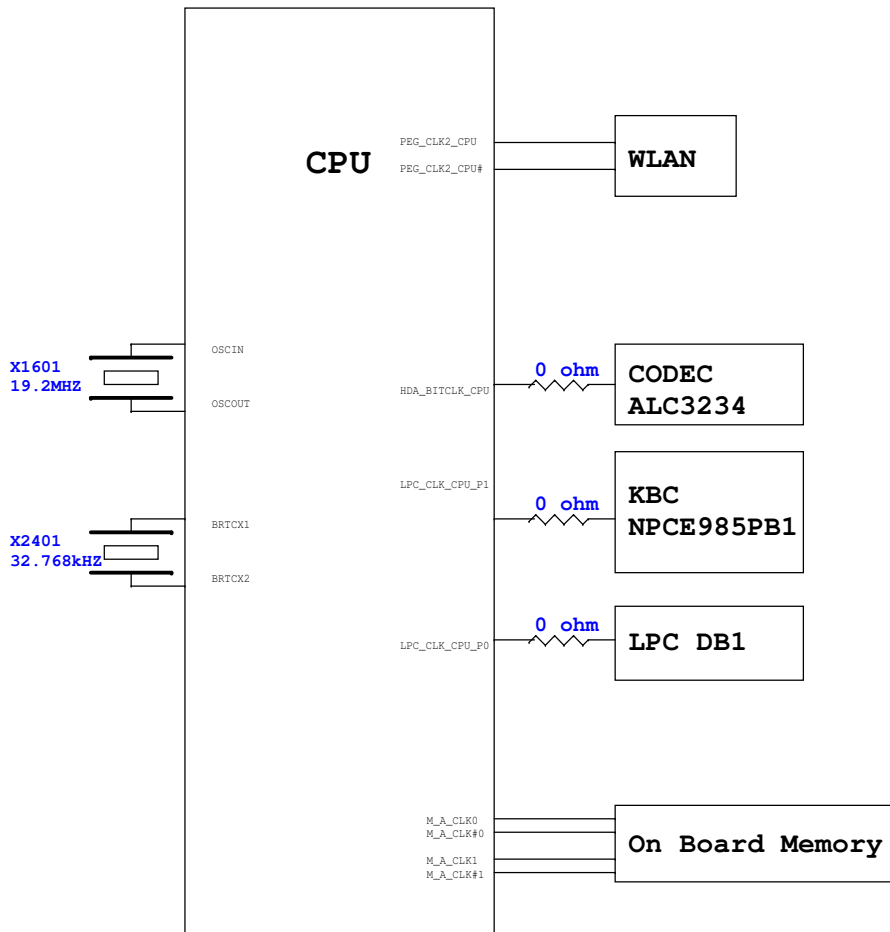
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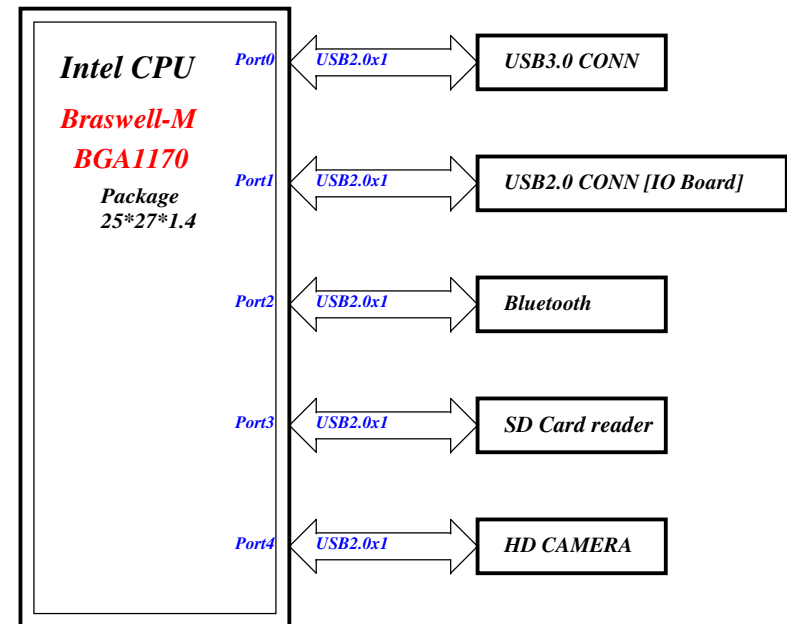
Audio Block Diagram



CLK Block Diagram



USB2.0 Port Block Diagram



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Title

CLK / SENSOR Block

Size
A3

Document Number

Rocket BSW 11.6"

Rev
A00

Date: Monday, November 09, 2015

Sheet 106 of 109

